新型雙開關主動箝位高升壓轉換器之研製

Implementation of a Novel High Step-Up Dual-Switch Active-Clamp Converter

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***Abstract*- In this paper, a series input parallel output high step-up voltage converter is proposed. This converter combines the forward converter and the flyback converter to achieve high step-up voltage when the switch is turned on. The topology is operated in symmetry. The two active switches are interleavedly controlled, and utilize the same clamp capacitor to achieve leakage energy recycling. The switches of the proposed converter achieve zero voltage switching (ZVS) at full load and middle load, on the other hand, they achieve low voltage switching at condition of lower load current. In this research, conventional high step-up voltage converters and related topologies are firstly introduced, followed by characteristic analysis and design of the proposed converter, which is verified by a prototype circuit in the laboratory with 24V input and 200 V/400W output.**

Keywords: leakage energy recycling, high step-up voltage, ZVS

摘　要

本文電路為輸入並聯、輸出串聯之高升壓轉換器，結合順向與返馳式轉換器，可於開關導通時具有電壓提升之特性，以提高轉換器之電壓轉換比。本架構轉換器為對稱性操作，二個主動開關為錯相式控制且共用同一箝位電容，並且利用此箝位電容達成漏電感能量回收。此轉換器開關在較大負載電流下，藉由共振使切換開關達成零電壓切換之特性，可降低開關之切換損失，另外，轉換器開關於較小負載電流條件下，切換開關則具有低電壓切換之特性。本文中將對常見之高升壓電路架構作簡介，並針對所提出之電路架構作特性分析與設計。最後，研製一輸入為 24 V，輸出為 200 V，輸出功率 400 W 之雛型電路以驗證理論分析之正確性。

關鍵字：漏感能量回收、高升壓、零電壓切換

I. INTRODUCTION

Due to energy lessen and the environmental protection has become a worldwide issue in the decades. Some green energy sources are invented, for examples, the solar photovoltaic power (PV power), the wind power, the fuel cells and the ocean power. Because the prosperity and the trend of green energy, many firms are devoted to research the green energy around the world. For these green energies, the voltages generated from them are low. Therefore, the systems' output voltage should be lifted up to a desired voltage we need to connect to utility by high step-up converters. High step-up converters are widely used in the front-end of green energy systems, uninterruptible power supplies (UPSs), batteries for the telecommunications industry and high intensity discharge lamps (HID) of vehicles headlamps. For example, the output voltage of the fuel cell system is 24~ 40V. When the system is connected to utilities, the output voltage of the system should be lifted to 200V or 400V so a step-up DC-DC converter will be required.

In conventional switching power suppliers, boost converters are suitable for voltage step-up applications because of their simple structure and high efficiency, so conventional boost converters are theoretically able to achieve high step-up voltage gains in large duty ratio. However, it is difficult in practice to achieve high step-up gains due to the equivalent series resistance (ESR) of elements. Besides, with very large duty ratio, the output rectifier will cause serious reverse recovery problems that the switch-off losses on the rectifier diode will degrade the efficiency and the electromagnetic interference (EMI) problem will also occur [1].

The newly proposed high step-up converters and techniques in recent years are voltage lift technique [2], switched-capacitor converter [3], coupled-inductor technique [4], cascade topology [5] and cascode topology [6]. Coupled-inductor technique is a widely-applied topology; however, the leakage inductor causes the voltage rating of the switch increases, hence degrades the efficiency of the converter. If the leakage energy is recycled and the reverse recovery problem of the output diode can be solved, the efficiency of the converter is improved.

At high power application, the current stress and conduction losses increase. For this reason, interleaved topology is proposed [7]. The feature of the interleaved topology is that the switches are symmetrically operated which share the current. Therefore, the conduction losses are reduced.

In this paper, a novel high step-up dual-switch active-clamp converter which is composed of the features of active-clamp and the cascode technique is proposed. The proposed topology has two converters which are interleavedly operated. Therefore, the two converters share the output power. In order to increase the voltage conversion ratio, the converters are series connected in the secondary side.

The basic operation process, characteristics and design principles will be analyzed in detail. Then experimental results are presented, which illustrate the converter function and verify the analysis presented.

II. THE PROPOSED CONVERTER

A. *Circuit description*

The proposed high step-up dual-switch active-clamp converter consisting of two forward-flyback converters, the forward-flyback_1 and the forward-flyback_2, is shown in Figure 1. The two converters are series input parallel output connected. Moreover, a clamp capacitor, C_C is added between two switches to clamp the voltage of switches; meanwhile, this capacitor is utilized to recycle the leakage energy. The forward-flyback_1 consists of S_1, T_1, D_1, D_2, C_1 and C_2 while the forward-flyback_2 consists of S_2, T_2, D_3, D_4, C_3 and C_4.

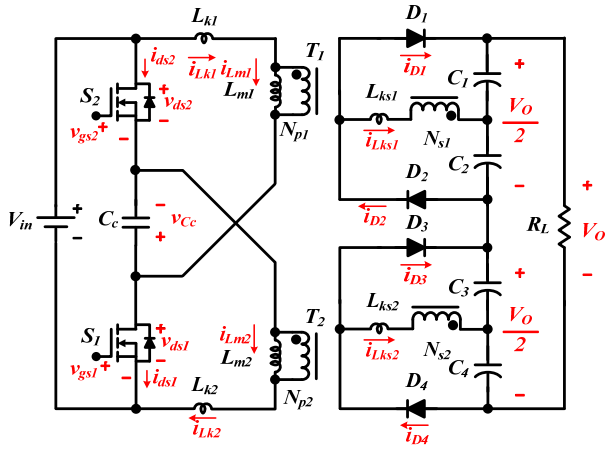


Figure 1 Proposed converter

III. OPERATING PRINCIPLE

In order to simplify the steady state analysis, the following assumptions are made.

1. Switches S_1 and S_2 are ideal.
2. Diodes D_1, D_2, D_3 and D_4 are ideal.
3. Transformers T_1 and T_2 are identity, so $n = \frac{N_{p1}}{N_{s1}} = \frac{N_{p2}}{N_{s2}}$.
4. Capacitors C_1, C_2, C_3 and C_4 are large enough that the voltage applied to the capacitors are constant voltage source.
5. The control signal, v_{gs1} and v_{gs2} are interleaved control.
6. All ESR of the components are neglected.

The proposed circuit has twelve distinct operating intervals in one period. Since the converter operation is symmetrical in each half cycle, only six intervals in half a period are discussed. The main waveforms of the proposed converter in boost mode are given in Fig. 2.

A. *Mode analysis*

Mode I ($t_0 \le t < t_1$): In mode I, v_{gs1} is high while v_{gs2} is low. S_1, D_2 and D_3 are conducted when S_2, D_1 and D_4 are off. The current path of this mode is shown in Figure 3(a). The operating principle of this mode is described as follows.

L_{m1} and L_{k1} are stored energy linearly by V_{in} and because i_{Lk1} is larger than i_{Lm1}, the energy of V_{in} is transferred to C_2 through T_1 and D_2. On the other hand, energy on L_{k2} is transferred to the clamp capacitor C_C. And the energy stored on the L_{m2} is transferred to C_3 through T_2 and D_3. When $t = t_1$, i_{Lk2} decreases to zero and the voltage on the clamp capacitor C_C, v_{Cc} reaches its peak value. When $t = t_1$, this mode ends.

Mode II ($t_1 \le t < t_2$): In mode II, v_{gs1} is high while v_{gs2} is low. S_1, D_2 and D_3 are conducted with S_2, D_1 and D_4 are turned off. The current path of this mode is shown in Figure 3(b). The operating principle of this mode is described as follows.

The energy of V_{in} is transferred to C_2 through T_1 and D_2. When $i_{Lk2} = 0$, the energy charged on the clamp capacitor C_C and the energy stored on the L_{m2} are transferred to C_3 through T_2 and D_3. When $t = t_2$, S_1 is turned off, this mode ends.

Mode III ($t_2 \le t < t_3$): In mode III, v_{gs1} and v_{gs2} are both low. D_2 and D_3 are conducted while S_1, S_2, D_1 and D_4 are off. The current path of this mode is shown in Figure 3(c). The operating principle of this mode is described as follows.

The energy stored on the L_{k1}, whose leakage energy is recycled, is transferred to C_C. Moreover, the energy of L_{k1} is transferred to C_2 through T_1 and D_2. On the other hand, current i_{Lk2} keeps flowing reversely, and the energy stored on the L_{k2} and L_{m2} are transferred to C_3 through T_2 and D_3 though a portion of the leakage energy of L_{k2} is also transferred back to V_{in}. When $t = t_3$, $i_{Lk2} = 0$, this mode ends.

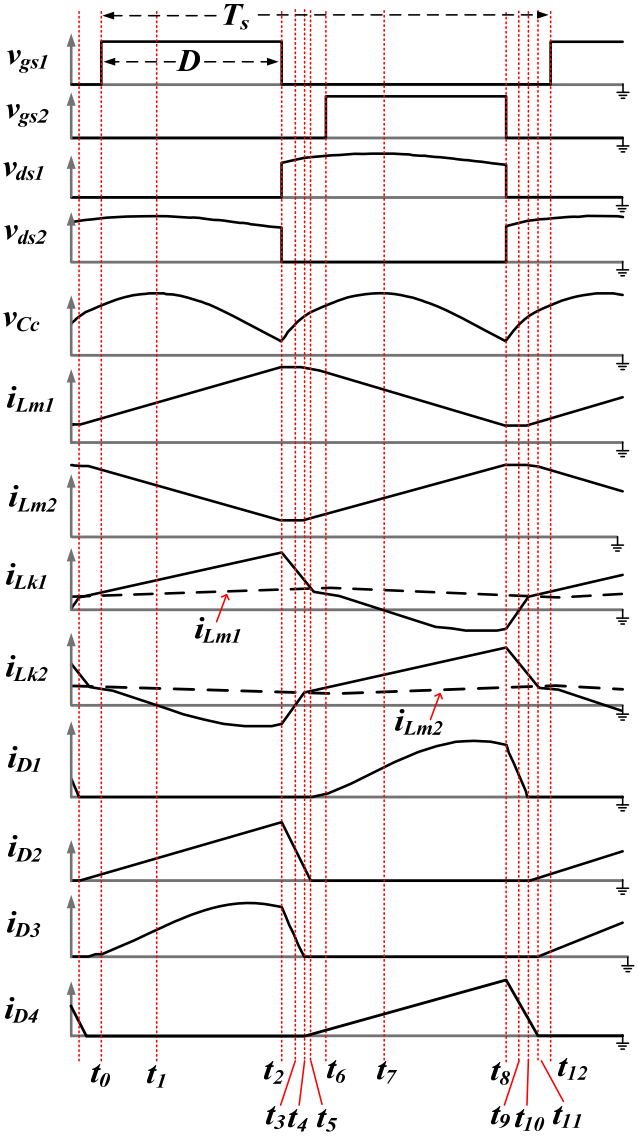


Figure 2 Key waveforms of the proposed converter

Mode IV ($t_3 \le t < t_4$): In mode IV, v_{gs1} and v_{gs2} are both low. D_2 and D_3 are conducted as S_1, S_2, D_1 and D_4 are off. The current path of this mode is shown in Figure 3(d). The operating principle of this mode is described as follows.

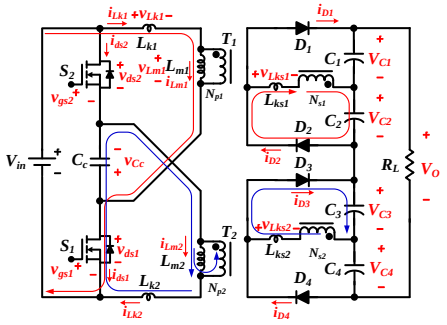
The energy stored on the L_{k1} is transferred to C_C and L_{k2}. The leakage energy can be recycled. Moreover, the energy of L_{k1} is transferred to C_2 through T_1 and D_2. The energy stored on the L_{m2} is transferred to C_3 through T_2 and D_3. On the other hand, L_{k2} is stored energy by V_{in} and i_{Lk1}. When $t = t_4$, $i_{Lk2} > i_{Lm2}$, this mode ends.

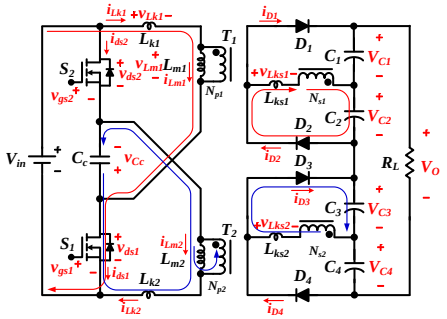
Mode V ($t_4 \le t < t_5$): In mode V, v_{gs1} and v_{gs2} are both low. D_2 and D_4 are conducted; S_1, S_2, D_1 and D_3 are off. The current path of this mode is shown in Figure 3(e). The operating principle of this mode is described as follows.

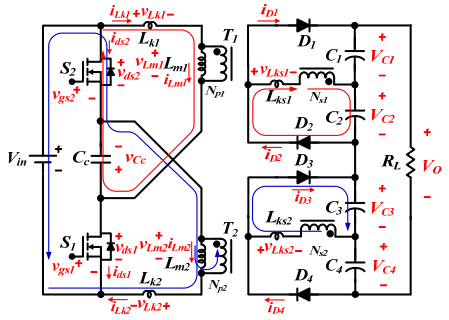
The energy stored on the L_{k1} is transferred to C_C. The leakage energy is recycled. Moreover, the energy of L_{k1} is transferred to C_2 through T_1 and D_2. Current i_{Lk2} keeps flowing, and the energy of V_{in} is transferred to C_4 through T_2 and D_4. In the same interval, the energy of V_{in} is transferred to L_{m2} and L_{k2}. When $t = t_5$, $i_{Lm1} > i_{Lk1}$, this mode completes.

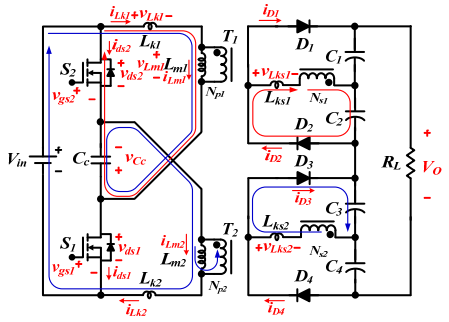
Mode VI ($t_5 \le t < t_6$): In mode VI, v_{gs1} and v_{gs2} are both low. D_1 and D_4 are conducted under the circumstance that S_1, S_2, D_2 and D_3 are off. The current path of this mode is shown in Figure 3(f). The operating principle of this mode is described as follow.

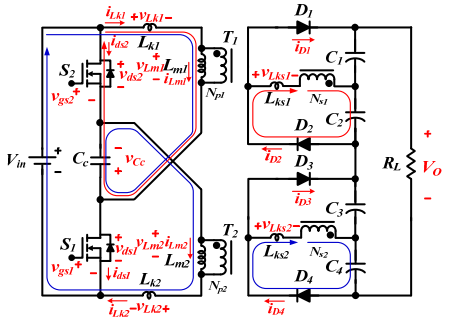
The energy stored on the L_{k1} is transferred to C_C. The leakage energy can be recycled. Moreover, the energy of L_{m1} is transferred to C_1 through T_1 and D_1. Current i_{Lk2} keeps flowing, and the energy of V_{in} is transferred to C_4 through T_2 and D_4. In the same interval, the energy of V_{in} is transferred to L_{m2} and L_{k2}. When $t = t_6$, S_2 is turned on, which puts this mode to an end.











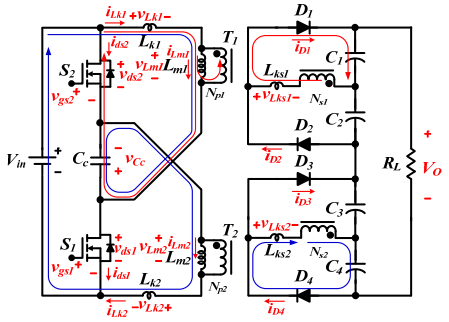


Figure 3 Operation modes of (a) Mode I, (b) Mode II, (c) Mode III, (d) Mode IV, (e) Mode V and (f) Mode VI for the proposed converter

IV. ANALYSIS OF THE PROPOSED CONVERTER

A. Voltage conversion ratio

In order to simplify the analysis, the effects of leakage inductors are neglected. Moreover, from the converter is symmetry operating. Thus, only the single converter, forward-flyback_1 is taken into analysis. The simplified model is shown in Figure 4.

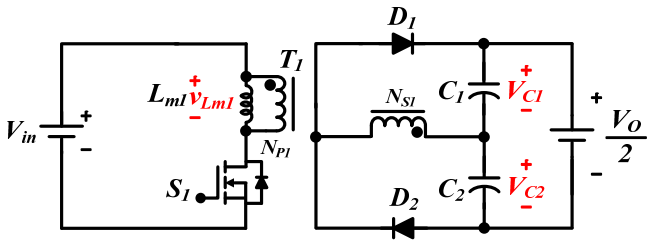


Figure 4 Simplified model of single converter

Ideally in CCM, when S_1 is turned on, V_{in} charges C_2 and the voltage of C_2 and L_{m1} are as follows:

$$V_{C2} = \frac{V_{in}}{n} \quad (1)$$

$$v_{Lm1} = V_{in} \quad (2)$$

Because forward-flyback_1 and forward-flyback_2 are identity, V_{C2}=V_{C4}. When S_1 is turned off, D_1 is conducted, the voltage of L_{m1} is:

$$v_{Lm1} = -n \cdot V_{C1} \quad (3)$$

By the volt-second balance theorem, the voltage relationship of L_{m1} is:

$$V_{in} \cdot D \cdot T_S = n \cdot V_{C1} \cdot (1-D) \cdot T_S \quad (4)$$

From Eq. (3.32), the voltage of C_1 is:

$$V_{C1} = \frac{D \cdot V_{in}}{n \cdot (1-D)} \quad (5)$$

Because forward-flyback_1 and forward-flyback_2 are identity, V_{C1}=V_{C3}.

From Figure 4, the output voltage of the single converter is determined by:

$$\frac{V_O}{2} = V_{C1} + V_{C2} \quad (6)$$

From Eq. (1), (5) and (6), the voltage conversion ratio of the proposed converter is:

$$\frac{V_O}{V_{in}} = \frac{2}{n \cdot (1-D)} \quad (7)$$

B. Voltage rating of power devices

According to Figure 5, when S_1 is turned on, D_2 is conducted. The voltage of v_x point is $-V_F$, which is the forward-voltage of the diode. The voltage stress of D_1 is:

$$v_{D1} = \frac{V_O}{2} - (-V_F) = \frac{V_O}{2} + V_F \quad (8)$$

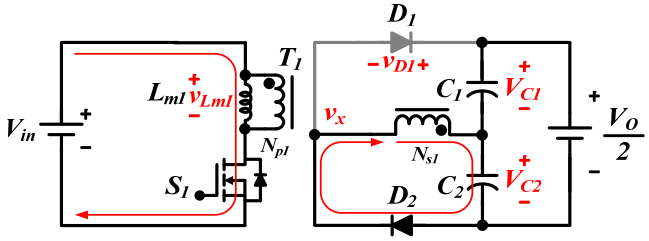


Figure 5 Simplified single converter when S_1 is on

According to Figure 6, when S_1 is turned off, D_1 is conducted. The voltage of v_x point is:

$$v_x = \frac{V_O}{2} + V_F \quad (9)$$

At the same time, the voltage of v_{D2} equals to v_x, therefore, v_{D2} has the same voltage rating as v_{D1}. The rectifier diodes of the other forward-flyback converter have the same voltage rating as v_{D1} and v_{D2}:

$$v_{D1} = v_{D2} = v_{D3} = v_{D4} = \frac{V_O}{2} + V_F \quad (10)$$

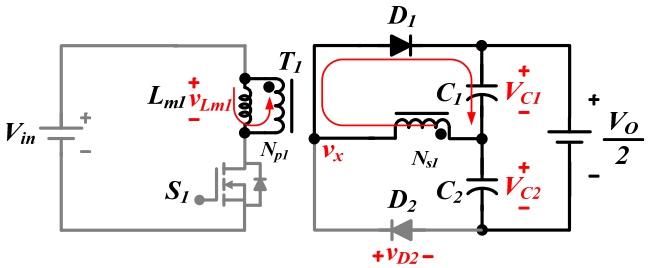


Figure 6 Simplified single converter when S_1 is off

V. CIRCUIT DESIGN

A. Turns ratio design

From Eq. (7) the turns ratio of the transformer can be calculated as:

$$n = \frac{2 \cdot V_{in}}{(1-D) \cdot V_O} \quad (11)$$

B. Magnetizing inductor L_m design

For a single forward-flyback converter, it only deals with half the power of the system, the output of each forward-flyback converter is 100 V. By the formula for designing the transformer of flyback converter [8-9], the L_m is:

$$L_m = \frac{(V_{in} \cdot D)^2}{2 \cdot V_O \cdot I_{BCM} \cdot f_s \cdot D} \quad (12)$$

C. Transformer Design

The primary winding turns of the transformer is:

$$N_p = \frac{L_m \cdot I_{L_{m,peak}}}{\Delta B_m \cdot A_e} \text{ Turns} \quad (13)$$

The turns number of the secondary winding N_s is:

$$N_s = \frac{N_p}{n} \text{ Turns} \quad (14)$$

D. Output Capacitors Design

When S_1 is turned on, the output current flows out of the output capacitor C_1, thus minimum of output capacitor C_1 is:

$$C_1 = \frac{\Delta Q_1}{\Delta V_{C1}} = \frac{I_O \cdot D \cdot T_S}{\Delta V_{C1}} \quad (15)$$

When the S_1 is turned off, the output current flows out of the output capacitor C_2, thus the minimum of output capacitor C_2 is:

$$C_2 = \frac{\Delta Q_2}{\Delta V_{C2}} = \frac{I_O \cdot (1-D) \cdot T_S}{\Delta V_{C2}} \quad (16)$$

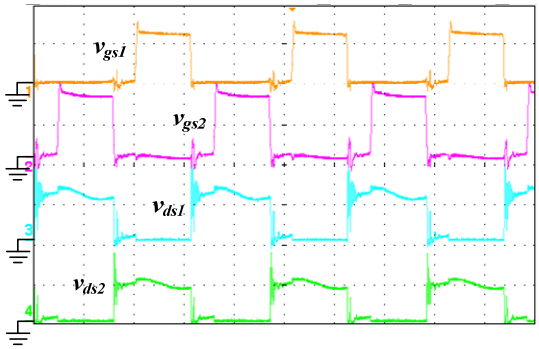
VI. EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, a 400W prototype converter is built and tested in the laboratory. The implementation of the proposed dual-switch

active-clamp converter is shown in Fig. 4. The experimental results are obtained with the following parameters.

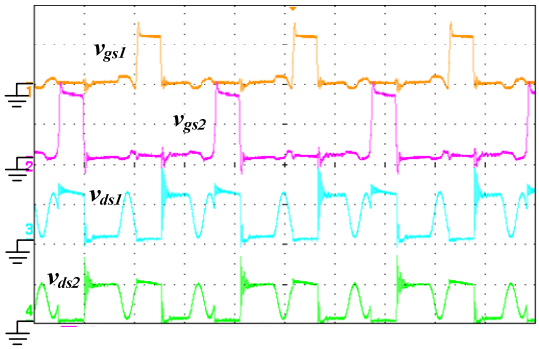
Output voltage: 200 V.
Output voltage ripple: 2 V.
Rated output current: 2 A.
Minimum output power for CCM operation: 400 W.
Switching frequency: 65 kHz.
Duty cycle: 0.4.
Output capacitance: 100 μF.

The experiment results for the prototype circuit are recorded in this section. Figure 7 and Figure 8 show the relationship between gate signals and the voltage across the drain and source of the switches under different load current conditions. Figure 9 and Figure 10 show the relationship between gate signals and the current flow through the two switches under different load current conditions. In addition, the voltages across the clamp capacitor under different load current conditions are shown in Figure 11 and Figure 12. Finally, output voltage is shown in Figure 13.



(ch1: 10V/div; ch2: 10V/div; ch3: 40V/div; ch4: 50V/ div; Time: 5us/div)

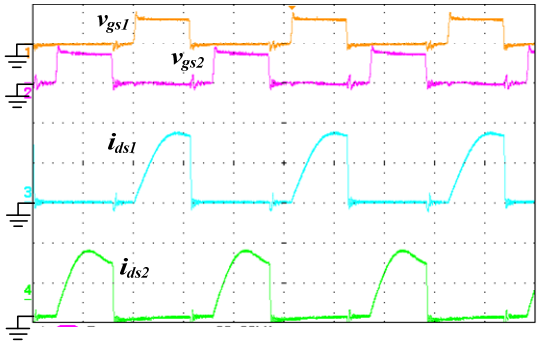
Figure 7 Measured waveforms of v_{gs1}, v_{gs2}, v_{ds1} and v_{ds2} at full load



(ch1: 10V/div; ch2: 10V/div; ch3: 40V/div; ch4: 50V/ div; Time: 5us/div)

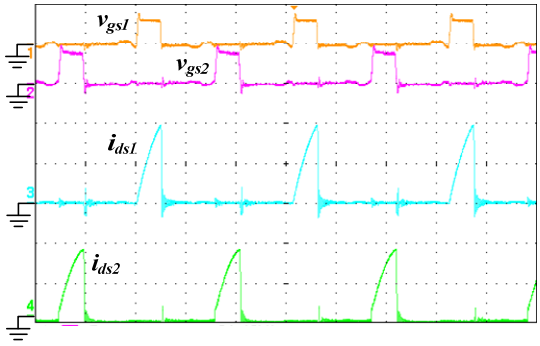
Figure 8 Measured waveforms of v_{gs1}, v_{gs2}, v_{ds1} and v_{ds2} at 20% load

The drain to source voltage was nearly identical to what is predicted by theory. From the above two figures, it can be seen that prototype circuit is operated under interleaved control. In addition, when the prototype circuit operated at full load, ZVS is achieved. On the other hand, when at light load, the switches only achieve low voltage switching. Finally, the voltage spikes of the switches are caused by trace amounts of inductor material on the PCB.



(ch1: 20V/div; ch2: 20V/div; ch3: 20A/div; ch4: 20A/ div; Time: 5us/div)

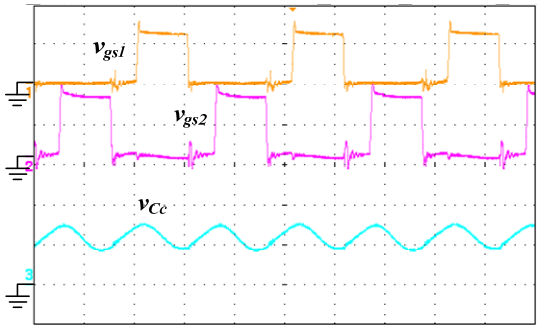
Figure 9 Measured waveforms of v_{gs1}, v_{gs2}, i_{ds1} and i_{ds2} at full load



(ch1: 20V/div; ch2: 20V/div; ch3: 10A/div; ch4: 10A/ div; Time: 5us/div)

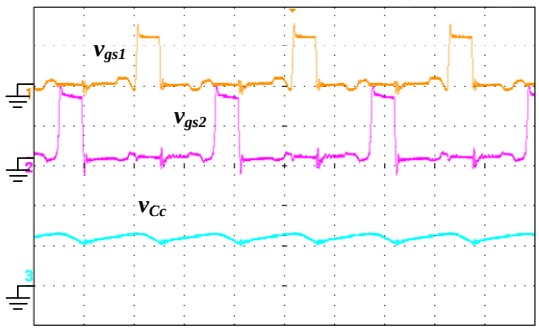
Figure 10 Measured waveforms of v_{gs1}, v_{gs2}, i_{ds1} and i_{ds2} at 20% load

The values predicted by theory and the measurements are similar to each other. The current flowing through the switch is much higher at full load than the light load. It is because at full load, the inductor is stored more energy. The decreasing interval of i_{ds1} and i_{ds2} in Figure 9 reveals the energy stored on the inductors is transferred to C_C.



(ch1: 20V/div; ch2: 20V/div; ch3: 20V/div; Time: 5us/div)

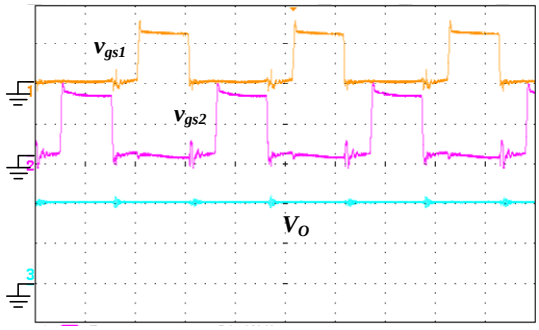
Figure 11 Measured waveforms of v_{gs1}, v_{gs2} and v_{Cc} at full load



(ch1: 20V/div; ch2: 20V/div; ch3: 20V/div; Time: 5us/div)

Figure 12 Measured waveforms of v_{gs1}, v_{gs2} and v_{Cc} at 20% load

Because the energy transferred to clamp capacitor C_C at light load is much less than that at full load. As a result, the peak to peak value on the clamp capacitor, $v_{Cc,pk\text{-}pk}$ ranked as: $v_{Cc,pk\text{-}pk}$ full load > $v_{Cc,pk\text{-}pk}$ light load.



(ch1: 20V/div; ch2: 20V/div; ch3: 100V/div; Time: 5us/div)

Figure 13 Measured waveforms of v_{gs1}, v_{gs2} and V_O at full load

The output voltage is shown in Figure 13 almost equals to the theory value. The voltage is almost a constant value, except the noise when the switches are turned off.

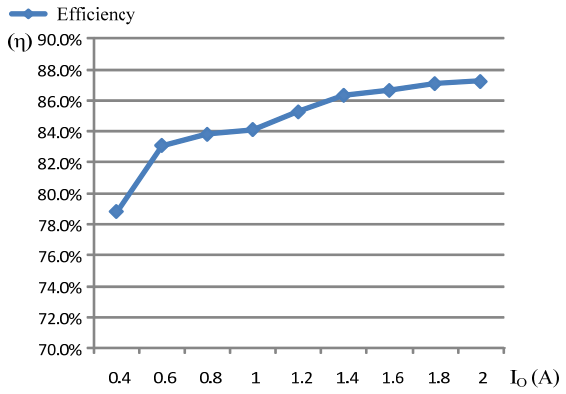


Figure 14 Efficiency curve of the prototype circuit

The efficiency curve of the prototype circuit can be illustrated in Figure 14. It is obvious that the maximum efficiency is 87% at full load. The minimum efficiency is 78.8% when output current I_O = 0.4A. The average efficiency is about 83%.

VII. CONCLUSIONS

In this paper, a series input parallel output high step-up voltage converter combined with leakage energy recycling techniques is proposed. The converter is operated in interleaved topology. For this reason, the input current is shared by two sub circuits and the conduction losses are reduced. In addition, a clamp capacitor is added to the circuit to recycle leakage energy. The switches of the proposed converter achieve zero voltage ZVS at full load, they achieve low voltage switching at lower load current. A prototype circuit with 24V input and 200 V/400W output is made to verify the proposed topology. By experiments, the ZVS and high step-up voltage features are proven feasible. Moreover, the leakage energy recycling is also verified to be correct.

In summary, the proposed converter can be used in the front-end of a green energy system.

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