A charge pump circuit -- cascading high-voltage clock generator

Wen Chang Huang\(^1\), Jin Chang Cheng\(^2\) and Po Chih Liou\(^1\)

\(^1\)Department of Electronic Engineering, Kun Shan University, Tainan, Taiwan, R.O.C.
\(^2\)Department of Accounting and Information System, Chang Jung Christian University, Tainan, Taiwan, R. O. C.

wchuang@mail.ksu.edu.tw

Abstract

A high efficiency charge pump circuit which is realized by multi-staged high-voltage clock (HVC) generator is presented. The ten-staged HVC charge pump circuit could pump the voltage up to 21.35\text{V} at a supply voltage of 2\text{V} in 0.35\mu m CMOS process. It also shows that the clock voltage increased linearly as the stages of the high-voltage clock generator was increased. No saturation tendency of the pumping voltage was observed after the ten-stage of pumping.

1. Introduction

Charge pumps are circuits that generate a voltage larger than the regular supply voltage from which they operate. Charge pumps have been used in the nonvolatile memories, such as EEPROM and flash memories, for the programming of the floating-gate devices [1,2]. They can also be used in the low-supply-voltage circuits and switched-capacitor systems that require high voltage to drive the analog switches [3]. Analog circuitry also requires efficient charge pump to augment the internal voltage supplies in order to achieve the increased dynamic range and simplify the design [4].

The charge pump circuit reported by Dickson has been widely used for generating high voltages [5,6]. The specific circuit makes use of capacitors, which are interconnected by diodes and coupled in parallel with two non-overlapping clocks. Diodes in the Dickson circuit can be replaced by NMOS, which will result a more practical implementation [7]. Fig. 1 shows a four-stage Dickson charge pump circuit. However its performance is limited due to the threshold voltage drop of the NMOS devices and the reverse charge-sharing phenomenon. Moreover, for high output generated voltages, the increase in the threshold voltage due to the body effect can significantly reduce the pumping efficiency.

In order to overcome the problems mentioned above in the Dickson charge pump, a charge pump, called NCP-2[8], is reported recently which utilizes the charge transfer switches (MSi transistors). Each of the MSi transistors is controlled by the pass transistors MNi and MPi as shown in Fig. 2. In that way the charge transfer switches can be turned off completely when required, preventing the reverse charge flow. Also they can be turned more effectively by the high voltage generated in the next stage.

Figure 1 A four-stage Dickson charge pump.

Figure 2 The NCP-2 charge pump circuit.
Figure 3 The proposed charge pump circuit—a chained of four-staged high-voltage clock (HVC) generator.

More complicated circuit scheme for charge pump have been applied to increase the voltage gain, such as all PMOS charge pump for low voltage operation [9], CMOS charge pump [10], charge transfer switches in combination with pumping the output stage clock of enhanced voltage amplitude [8]. In this paper, a new charge pump scheme is discussed. The high-voltage clock generator is used to generate the clock voltage for the next stage. Based upon this concept, multistage of the high-voltage clock generator of up to ten stages is designed.

2. Proposed new charge pump circuit — HVC charge pump

The proposed charge pump circuit is shown in Fig. 3. It can generate a higher output voltage than the circuits mentioned above. Each stage of the new charge pump circuit is based on the structure of high-voltage clock generator and the output voltage of the previous stage is applied to be the clock voltage of the next stage. The supply voltage of each stage is constant at $V_{DD}$. A four stage connection of the high voltage clock (HVC) generated charge pump circuit is shown in Fig. 3. The operation of the high-voltage clock generator is described in sections 2.1 and the concept of multistage of the clock voltage doubler is discussed in section 2.2. The simulation results of the proposed high-voltage clock generated charge pump circuit are shown in section 2.3.

2.1. Voltage doubler

Basically, the high-voltage clock generator is a voltage doubler. Fig. 4 shows a conventional voltage doubler [8]. Both the supply voltage and the clock voltage, $V_{CLK}$, of the voltage doubler are $V_{DD}$. It operates as follows: during $V_{CLK}=V_{DD}$, transistor $M_1$ turns off, transistor $M_2$ turns on and capacitor $C_2$ is charged to $V_{DD}$. During $V_{CLK}=V_{DD}$, transistor $M_4$ on, transistor $M_5$ turns off and capacitor $C_1$ is charged to $V_{DD}$. Capacitor $C_2$, which is charged to $V_{DD}$ during the previous clock phase, is now lifting the output voltage $V_{out1}$ to $2V_{DD}$. Eventually, the output voltage $V_{out1}$ is $2V_{DD}$ during $V_{CLK}=V_{DD}$ and is $V_{DD}$ during $V_{CLK}=0$ at steady state. Similarly, the output voltage $V_{out2}$ is $V_{DD}$ during $V_{CLK}=V_{DD}$ and is $2V_{DD}$ during $V_{CLK}=0$. The timing diagrams of the voltage doubler are also shown in Fig. 4.
As mentioned above, the output voltage is increased and changed between $V_{DD}$ and $2V_{DD}$ in the conventional voltage doubler during clocking. In order to obtain a clock scheme which the amplitude of its voltage is oscillated between 0V and $2V_{DD}$, a CMOS inverter is added to each node of the output, as shown in Fig. 5. The circuit was named clock voltage doubler [11]. In the circuit, the output node out1 is connected to the source end of the PMOS (M5) of the inverter, and the gate of the CMOS inverter (M5 and M6) is controlled by $V_{CLK}$. Likewise, the output node out2 is connected to the source end of M7, and the gate of the CMOS inverter (M7 and M8) is controlled by $V_{CLK}$. The operation of the circuit is described as follow. During $V_{CLK}=V_{DD}$, as discussed above, out1 is $2V_{DD}$, the gate voltage of the CMOS inverter (M5 and M6) is 0V, M5 turns on, M6 turns off and the output voltage of V out3 is charged to $2V_{DD}$. During $V_{CLK}=0$, out1 is $V_{DD}$, the gate voltage of CMOS inverter (M5 and M6) is $V_{DD}$, so M5 turns off, M6 turns on and the output voltage of V out3 is discharged to 0V. The same principle of operation also occurs at the right hand part of the circuit. Eventually, during $V_{CLK}=V_{DD}$ the node voltages of V out3 and V out4 are $2V_{DD}$ and 0V, respectively. And during $V_{CLK}=0$ the node voltages of V out3 and V out4 are switched to 0V and $2V_{DD}$, respectively. The timing diagrams of the output nodes out3 and out4 were illustrated in Figure 5.
2.2. Multi-stage high-voltage clock generator

Figure 6 shows the circuit of a four-stage high-voltage clock generator. In the first stage, the lower plate of the capacitor \( C_1 \) and \( C_2 \) are connected to the clock \( V_{CLK} \) and \( V_{CLK} \). The output node A is connected to the lower plate of the capacitor \( C_4 \) of the second stage and the output node B is connected to the lower plate of the capacitor \( C_3 \) of the second stage. The same rules are applied to the following stages. The supply voltage of each voltage is constant at \( V_{DD} \). The clock voltage is gradually increased stage by stage which due to the high-voltage clock generator.

Figure 7 shows the timing diagrams of the output node B of the first stage, of the output node D of the second stage and the output node F of the third stage. The input clock voltage is \( V_{DD} \), the output voltage of the first stage will reach to \( 2V_{DD} \), \( 3V_{DD} \) for the second stage’s output and \( 4V_{DD} \) for the third stage’s output. During \( V_{CLK}=V_{DD} \), the first stage shows voltages of \( 2V_{DD} \) for \( V_A \) and \( 0V \) for \( V_B \), the second stage shows voltages of \( 0V \) for \( V_C \) and \( 3V_{DD} \) for \( V_D \), and the third stage shows voltage of \( 4V_{DD} \) for \( V_E \) and \( 0V \) for \( V_F \) after steady state. During \( V_{CLK}=V_{DD} \), the first stage shows voltages of \( 0V \) for \( V_A \) and \( 2V_{DD} \) for \( V_B \), the second stage shows voltages of \( 3V_{DD} \) for \( V_C \) and \( 0V \) for \( V_D \), and the third stage shows voltage of \( 0V \) for \( V_E \) and \( 4V_{DD} \) for \( V_F \) after steady state.

Figure 8 shows the simulation results of each stage’s output voltage (voltage high of the clocking voltage) of a ten-stage high-voltage clock generator. It shows that the output clock is pumped to \( 2V \) at stage-one’s output and is pumped to \( 11V \) at the output of the 10th stages.
2.3. Simulation results of the high-voltage clock generated charge pump circuit (HVC-charg pump)

A four stage high-voltage clock generated charge pump circuit is shown in Fig. 3. The stages of HVC-charg pump circuit which is simulated up to ten stages in the research. The nMOS diode is used to transfer the clock voltage into a steady dc voltage at the output of each stage. The simulation result of the pumping voltage of each stage is shown in Fig. 9. The supply voltage, $V_{DD}$, and the initial clock voltage, $V_{CLK}$ are 2V. The pumping voltage is up to 3.5V for the output of the first stage’s clock generator. As the number of stages is increased, the output voltage is increased steadily. The pumping voltage can be reached to 21.35V at the output of the 10th stage that is shown in the figure. Fig. 10 shows a comparison of the pumping voltage for various charge pump circuits. It shows that the HVC-charg pump has a better pumping voltage than others. For example, after twelve capacitors pumping (six stages in HVC), the output of NCP-1 is 11.3V, of NCP-2 is 9.3V while the HVC can reach up to 13.4V. Moreover, if the HVC was increased to ten stages, its output voltage can be reached to 21.35V. Also the HVC charge pump circuit does not show any tendency of saturation in the pumping voltage. The pumping voltage is increased linearly as the stage is increased.

3. Conclusion

A new charge pump circuit is proposed in this paper. Using multistage high-voltage clock generator,
the charge pump circuit can pump to an output voltage of 21.35V for a ten-stage design. The circuit also shows that the pumping voltage increases linearly as the pumping stage increases.

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5. References


