A 3.2-GHz Quadrature Signal Generator Based on a Single-Stage LC VCO in 0.25-μm CMOS Process

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doi:10.5729/amcm.vol1.issue1.28

Keywords: CMOS, LC voltage-controlled oscillator (VCO), Phase separator, Quadrature generator.

Abstract. This paper proposes a 3.2-GHz quadrature signal generator, which consists of a single-stage LC voltage-controlled oscillator (VCO) and a phase separator. The LC VCO consists of a PMOS cross-coupled pair and a parallel LC resonant circuit to achieve low phase noise. The phase separator consists of a three-stage RC quadrature network to mitigate the effect of process variation. The measured frequency of the free-running VCO is 3.19 GHz. The measured phase noise values from oscillator signals of 100-kHz and 1-MHz offset frequencies are -106.6 and -116 dBc/Hz, respectively. The measured frequency from the quadrature generator output is 3.18 GHz. The current consumption of the quadrature signal generator is 9 mA at a 2.5-V DC voltage. The quadrature signal generator is implemented in the TSMC 0.25-μm CMOS process with a total chip size of 0.98 × 0.99 mm2.

1. Introduction

The worldwide interoperability for microwave access (WiMAX) is a new form of broadband wireless access, which is based on the IEEE 802.16 standard [1], [2]. According to the standard, the frequency ranges of 2.3-2.7, 3.3-3.8, and 4.95-5.95 GHz included in the unlicensed Industrial-Science-Medical (ISM) band are adopted for WiMAX application. The development of WiMAX technology has drastically increased in recent years. WiMAX technology is expected to be cheaper than 3G on a per-bit basis and has the ability to deliver high-speed wireless internet access to the masses [3].

Generating a quadrature signal is an important technique in wireless transceiver applications [4], [5]. Several topologies for quadrature-signal generation have been proposed, including the quadrature voltage-controlled oscillator (QVCO) [6]-[8], an oscillator that operates at twice the required frequency with a frequency divide-by-two circuit [9], and an oscillator in series with a quadrature generator [10]. The QVCO usually uses two parallel-coupled VCOs to generate quadrature signals; however, it consumes high DC power and easily generates inaccurate quadrature signals due to an asymmetric duty cycle clock. The oscillator that operates at twice the required frequency with a frequency divide-by-two circuit offers a good match between simulated and measured oscillation frequencies and has a small chip area, with excellent quadrature accuracy feasible. However, it consumes extra power because of a frequency divider inserted in. In addition, dummy output buffers are required to ensure adequate symmetry.

In this paper, a 3.2-GHz CMOS quadrature signal generator is proposed, which can be applied to
WiMAX. A block diagram of the proposed quadrature generator is shown in Figure 1. The generator can be divided in two parts: a single-stage LC VCO and an accurate phase separator based on a three-stage RC network. Because the phase separator is composed of passive RC devices, it does not consume any DC power and reduces the phase noise in the circuit. The three-stage RC network is used to reduce the effect of process variation.

The rest of this paper is organized as follows. Section II introduces the circuit designs of the proposed LC VCO and the RC phase separator. Measurement results are discussed in Section III. Finally, conclusions are given in Section IV.

![Figure 1. Block diagram of the proposed quadrature signal generator](image1)

2. Circuit design

2.1 LC voltage-controlled oscillator design

Figure 2 shows a schematic of the proposed LC VCO. PMOS transistors M1-M4 create a cross-coupled connection which produces negative conductance to compensate for the losses of the LC resonant circuit. Transistors M3 and M4 in the cross-coupled circuit work as two common-drain circuits, providing sufficient output current to drive the quadrature generator at the next stage. The channel widths of transistors M1, M2 and M3, M4 are 70 and 90 μm, respectively. The current mirror, consisting of transistors M5-M7, supplies a bias current to the oscillator. The channel widths of transistors M5, M7 and M6 are 12 and 20 μm, respectively. The transistors of the oscillator circuit are all PMOS, which effectively reduces the phase noise.

The LC resonant circuit consists of two inductors (L1, L2) and two capacitors (C1, C2) in series with two MOS varactors (D1, D2). The inverted DC voltage (VCtrl) applied to the MOS varactors produces a capacitance-voltage dependence. Therefore, the oscillating frequency can be tuned by adjusting the voltage. The expression for the oscillating frequency for the proposed oscillator can be approximated as follows:

$$f_o = \frac{1}{2\pi \sqrt{L_i (C_f / C_D)}}.$$

where CD is the equivalent capacitance of the MOS varactors. For the proposed oscillator, the inductances (L1, L2) and the capacitances (C1, C2) are 3.715 nH and 0.55 pF, respectively.

![Figure 2. Schematic of the proposed LC VCO](image2)

2.2 Phase separator design

Figure 3 shows a schematic of the proposed phase separator. The circuit consists of a three-stage
RC quadrature network in series. Each stage includes four RC circuits, whose capacitors are connected to the resistor in the next RC circuit. The input differential signal is injected to the first stage of the quadrature circuit, where the upper and lower parts of the two resistors are connected together. The generator outputs are then connected to buffers, which are composed of common-source amplifiers, to produce sufficient output power for driving a 50-Ω load. The resistance and capacitance in each RC circuit are 200 Ω and 0.33 pF, respectively, to achieve a 240-kHz resonant frequency.

Using the three-stage RC quadrature network can reduce process-variation effect on capacitors and resistors, so it provides better phase and amplitude matching. Figure 4 shows the simulated phase at the phase separator output with the resistor value varying by ±10 %. Good phase matching is exhibited at 3.2 GHz; the worst phase error is 5° over the frequency range of 1.75 to 4.5 GHz. Figure 5 shows the simulated output power for the phase separator with an injected -0.5-dBm input signal. Good amplitude matching is exhibited at a 3.2-GHz input frequency and the amplitude error is lower than 0.2 dBm over the entire frequency range.

![Figure 3. Circuit schematic of the proposed RC phase separator](image_url)

![Figure 4. Simulated phase at the phase separator output with resistor value varying by ±10 %](image_url)

![Figure 5. Simulated output power for the phase separator with an injected -0.5-dBm input signal](image_url)
3. Measurement results

The proposed LC VCO and the phase separator were simulated in the TSMC 0.25-um CMOS process using Agilent ADS. The chip was mounted on an FR-4 PCB and wire-bonded out for connection to a spectrum analyzer for the RF measurements. Figure 6 shows the die micrograph. The chip occupies an area of 0.98 × 0.99 mm².

The measured output spectrum of the VCO is shown in Figure 7. When the VCO was under the free-running condition, the output power was -7.49 dBm at 3.19 GHz. Figure 8 shows the phase noise measured at 100-KHz and 1-MHz offset frequencies from the oscillator signal; the phase noise values are -106.6 and -116 dBc/Hz, respectively. Figure 9 shows the measured output spectrum from the phase separator output. The frequencies are all equal to 3.18 GHz. The output power values at the I and Q ports are both -12 dBm. However, due to the effect of process variation for the phase separator, the output power values at the Ibar and Qbar ports are -7 and -20 dBm, respectively. The core circuit draws 9 mA at a 2.5-V DC voltage. Table I summarizes the performance of the proposed CMOS quadrature generator.

![Figure 6. Chip micrograph of the proposed quadrature signal generator](image)

![Figure 7. Measured output spectrum of the VCO](image)

![Figure 8. Measured phase noise at 100-kHz and 1-MHz offset frequencies from the oscillator signal](image)

Table I summarizes the performance of the proposed CMOS quadrature generator.
Table I. Performance summary of the proposed CMOS quadrature signal generator

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>22.5 mW</td>
</tr>
<tr>
<td>Frequency tuning range</td>
<td>3.19 - 4.09 GHz</td>
</tr>
<tr>
<td>Phase noise @ 1-MHz</td>
<td>-116 dBc/Hz</td>
</tr>
<tr>
<td>Process</td>
<td>0.25 μm</td>
</tr>
</tbody>
</table>

4. Conclusion

A 3.2-GHz CMOS quadrature signal generator which consists of a single-stage LC VCO in series with an RC phase separator was presented in this paper. The LC VCO, whose transistors are all PMOS, achieves low phase-noise performance. The phase separator, which uses a three-stage RC network in series, produces an accurate quadrature phase shift and is robust against process variation. The proposed quadrature generator is suitable for WiMAX application.

5. Acknowledgment

This work was partly supported by National Science Council (NSC) of Taiwan under grant NSC 98-2218-E-168-001. The authors would like to thank Chip Implementation Center (CIC) of the NSC for their support in the TSMC CMOS process.

References


