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Pt/Al stacked metals gate MESFET

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ABSTRACT

A new InP MESFET structure both with a gate structure of stacked metal and with a active channel of stacked layer is proposed. The gate metals are constituted by a double metal structure, Pt/Al. It improves the barrier height and reduces the reverse leakage current in the MFSFET. This is due to the formation of Al_2O_3, and becoming a Pt/Al/Al_2O_3/InP, metal-insulating-semiconductor structure in the gate region of the transistor. The conductive channel is constituted by a stack-layered structure, a n-InP layer and an i-InP layer. A transfer characteristics of excellent pitch off, and transconductance of 93 mS/mm is derived. It also shows a negative differential resistance effect on the MESFET. The illumination and temperature effect of the transistor are brought into discussed.

1. Introduction

InP is believed to be an attractive material for high frequency and high power electronic devices because it has high peak and saturation velocities of electrons, and high thermal conductivity [1]. Therefore, InP-based field-effect transistors (FETs) are potentially better than GaAs metal–semiconductor field-effect transistors (MESFETs). However, the direct fabrication of a good Schottky contacts on n-InP has not been possible because of the low Schotthy barrier height, approximately 0.3–0.4 eV [2]. This low Schottky barrier height should result large reverse leakage currents and limit the performance of the MESFETs.

In order to reduce such high gate leakage currents, many attempts have been developed. It has been proposed to place a dielectric, such as InP_xO_y, CdO_x and phosphorus nitride film etc., between gate metal and InP channel [3–12] to form an metal–insulator-semiconductor FETs (MISFETs). However, these MISFETs suffer from problem of drain current drift [6] owing to the existence of high density of interface states which continue to hinder the development of this technology. Another approach to obtain good InP MESFET characteristics is to perform surface treatment and passivation prior to the gate metal deposition [13,14]. Surface passivation techniques involving the growth of thin native oxides by thermal or wet chemical oxidation have been reported to increase the barrier height, and an n-channel InP FET with stable high-performance gates has been demonstrated. Also, large band gap heterojunction AlInAs/InP FETs and GaInP/InP FETs [15–17] have been fabricated, where the gate metal is deposited upon the AlInAs or GaInP layer to achieve a high Schottky barrier. Also, a stable InP MESFET with a buried planar doped P^{++} layer that enhanced the Schottky contact has been fabricated [18]. In this paper, we present a new depletion mode InP MESFET with a double-metal gate structure, Pt/Al [19] and a stack-layered conductive channel. The dc electrical characteristics of the device was studied in detail in this work.

2. Experimental

The cross-sectional view of the double-metal gate, Pt/Al, InP MESFET is shown in Fig. 1. Fe-doped semi-insulating InP substrate was used in the experiments. The epitaxial layers of a undoped i-InP layer, a Si doped n-InP active layer and a n^+-InP layer for ohmic contact were grown by metal–organic chemical vapor deposition system (MOCVD) in sequence. The thickness and doping concentration are 1000 Å and about 5–9 $\times$ 10^{15} cm^{-3} for the undoped i-InP layer, 2000 Å and 1 $\times$ 10^{17} cm^{-3} for n-InP layer and 500 Å and 2 $\times$ 10^{18} cm^{-3} for the ohmic n^+-InP layer, respectively. The process of the device fabrication began with a mesa etching by using H_3PO_4:H_2O_2 = 1:1 which etching to the semi-insulator InP substrate. Ohmic contacts were formed with evaporating Au(1500 Å)/Ge(500 Å)/Ni(300 Å) on the source and drain by using E-gun vacuum system, and obtained the patterns by using the lift-off process. The ohmicity of source and drain were obtained through rapid thermal annealing (RTA) at 400 °C for 10 s. After the gate pattern was defined photoligraphically, the channel region was recessed by using H_3PO_4:H_2O_2 = 1:1 with an etching rate of 100 Å/min. Gate metal composed of Pt(500 Å)/Al(85 Å) was deposited by E-gun evaporation system at the base pressure of

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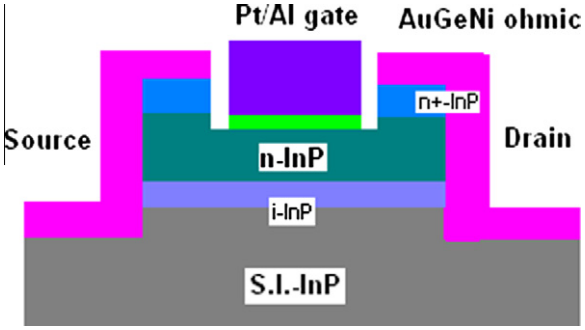

Fig. 1. The *I-V* characteristic of the 400 °C annealed Pt/Al/n-InP diode.

1×10^{-6} torr and then the gate metals were lifted-off. Device gate length with 0.5, 0.8, 1, 2 and 3 μm and gate width with 25, 50, 100 and 130 μm were fabricated, respectively. The specific contact resistance measurements were made using the transmission line model (TLM). The current–voltage (*I–V*) characteristics of the gate-to-source diode and *I–V* characteristics of MESFET were measured. The temperature and illumination effects were also discussed.

3. Results and discussion

3.1. Barrier height and specific contact resistance

The *I*–V characteristics of the Pt/Al gate-to-source diodes were measured at room temperature and analyzed on the basis of the thermionic emission model. The electrical characteristic of the Pt/Al/n-InP diode had been discussed [19]. The application of the stacked metals, Pt/Al to the gate of MESFET was realized in the study. The diode structure exhibits a effective barrier height of 0.7 eV, with an ideality factor of 1.11. The reverse leakage current is 2.6×10^{-7} Å at −3 V as shown in Fig. 2. The diode structure of the MESFET shows a better barrier height than that of conventional metal/n-InP diode. The source and drain of the transistor shows a reasonable contact resistance. The specific contact resistance of the source and drain contact is 1.06×10^{-5} Ω-cm^2. It was obtained from the TLM pattern of the sample.

The improvement of the barrier height of the Pt/Al/n-InP diode is due to the formation of aluminum oxide at the contact interface. The secondary ion mass spectrum (SIMS) of the annealed Pt/Al/n-InP diode had been discussed [19]. It shows the distribution of the elements Pt, Al, In, P and O. The element Pt was firstly detected on the sample. The element profiles of O and Al overlay was observed, and their peak signals are located between Pt and InP. Fig. 3 shows the X-ray diffraction (XRD) analysis of the Pt/Al/n-InP after it was RTA annealed at 400 °C for 30 s. In the spectrum, it shows the phase of Al_2O_3(1 1 0) which centered at $2\theta = 21.4°$. The metal phase of Pt and Al are still observed at the XRD spectrum. From the XRD and SIMS analysis of the Pt/Al/InP, it proofs the formation of Al_2O_3 at the contact interface. The formation of Al_2O_3 was due to the reaction between aluminum and oxygen. The oxygen came from the air of vacuum chamber and oxidant of the InP surface. For the diffraction peak of Al was still detected by XRD. It speaks for the aluminum was not fully consumed in the formation of aluminum oxide. The Pt/Al/n-InP contact scheme becomes Pt/Al/Al_2O_3/n-InP, metal–insulator-semiconductor structure. So the effective barrier is improved at the MESFET.

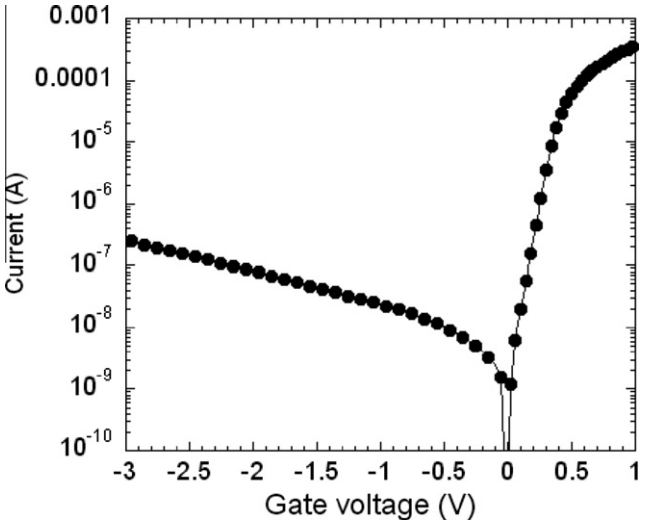

Fig. 2. The *I-V* characteristic of the 400 °C annealed Pt/Al/n-InP diode.

3.2. Transfer characteristics of MESFET

Fig. 4 shows the transfer characteristics (I_d versus V_{ds}) of the MESFET which with gate area of 2×50 μm. The characteristics demonstrated excellent channel pitch-off at a threshold voltage of −3 V. It shows good linear characteristics at low drain voltage region. At saturation region, the device shows negative resistance effect. For the curve of $V_{gs} = 0$ of the transfer characteristics, the drain current increased with the increasing of the drain voltage, while the drain current dropped suddenly about 1.2 mA at drain voltage of 2.4 V. The mechanism of the negative resistance effect will be discussed in next section.

Fig. 5 shows the extrinsic transconductance (g_m) and drain current (I_d) as a function of the gate-to-source voltage (V_{gs}) for the same device at the drain-to-source voltage (V_{ds}) of 1.5 V. The transconductance increases with the increase of gate voltage, it shows a peak value of 93 mS/mm at the gate bias of 1.1 V. The corresponding source resistance R_s is 50.

For a MESFET, the magnitude of the drain saturation current is dependent on the conductive channel layer. That is, it dependent on the thickness and carrier concentration of the conductive channel. As the thickness of the channel is increased, the cross section area of conductive channel would be increased. So the current flow

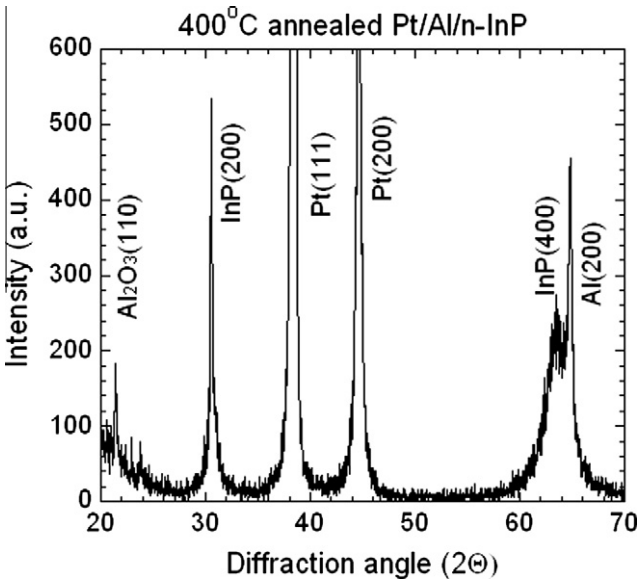

Fig. 3. The XRD analysis of the 400 °C annealed Pt/Al/n-InP diode.

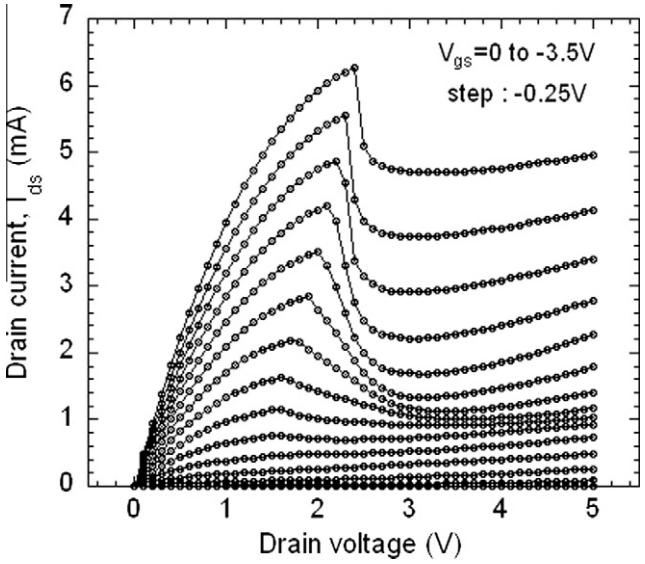

Fig. 4. The transfer characteristics of the double-metal gate, Pt/Al, InP MESFET.

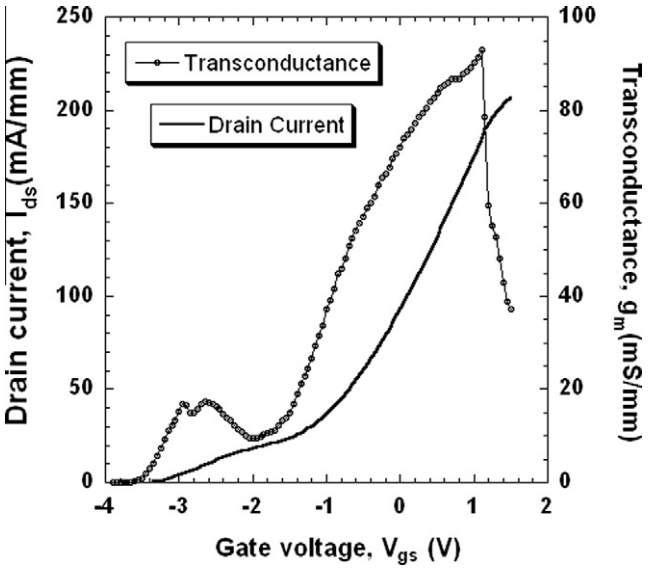

Fig. 5. The drain current and transconductance of the InP MESFET.

is increased. Also, the increase of carrier concentration in the channel would give rise to a higher level of drain saturation current. Now, the stack-layered conductive channel of this device is constituted by a 1000 Å i-InP layer and a 2000 Å n-InP layer. The undope-InP shows a carrier concentration of 5–9 $\times$ 10^{15} cm^{-3} and the n-InP has a carrier concentration of 1 $\times$ 10^{17} cm^{-3}. The thickness of the conductive channel of the n-InP layer was slightly etched before gate metal deposition. For the device, firstly the current was dominated by the n-InP layer with higher current level before the n-InP layer was depleted. While, as the n-InP layer was depleted, the current was dominated by the i- InP layer with lower current level. The gate depletion region increased toward channel layer as the drain to gate voltage (V_{DG}) is increased. That is, the n-InP channel layer would be depleted firstly, and then the i-InP layer. A higher current level was shown in the transfer characteristics before the n-InP was fully depleted. While, the drain would decrease to a lower current level suddenly, as the n-InP layer was completely depleted. So it shows a negative resistance effect during the increasing of the drain voltage.

From the observation of drain current (I_d) and source current (I_s) versus drain voltage (V_{ds}) characteristics of the transistor, as shown in Fig. 6. It shows that the drain current was the same with the source current before the depletion region reached to the i-InP layer. After it reached to the i-InP layer, the source current was controlled by the doping of the channel on the source end, and the source current decreased. For a further increase of the drain voltage, it shows the source current slightly larger than the drain current. It means some of the source current does not reach to the drain end. Fig. 7 shows the gate current and drain current of the InP MESFET during the applying of drain voltage. It shows current difference between source current and drain current becomes gate leakage current.

3.3. Illumination and temperature effect

Fig. 8 shows the transfer characteristics of the device with and without illumination, respectively. Due to the existence of gate, drain and source metal, only the regions which between gate and source and between gate and drain are illuminated. The resistance in these regions decreased, so the current increased in all curves. The carrier concentration under gate region is unchanged, so the

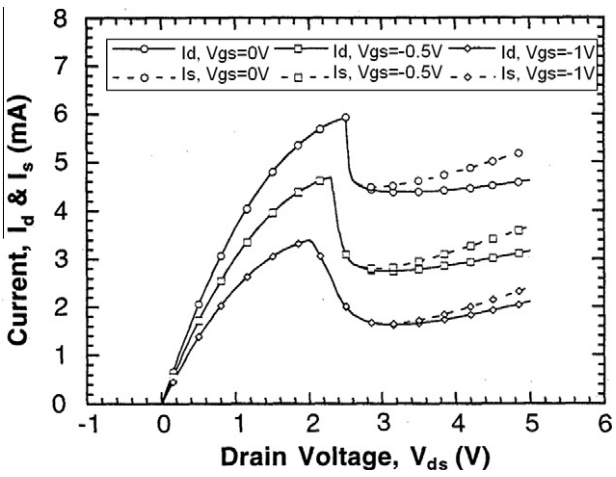

Fig. 6. The drain current (I_d) and source current (I_s) versus drain voltage (V_{ds}) characteristics of the InP MESFET.

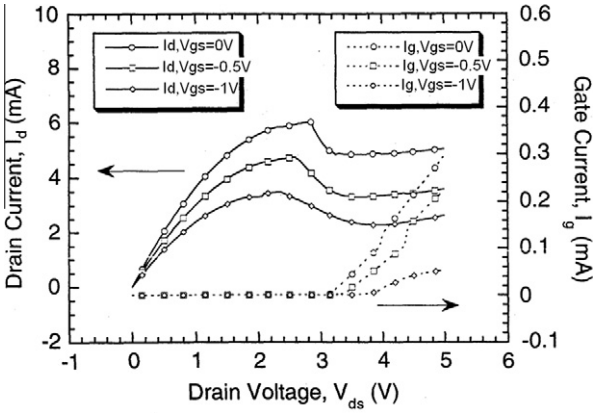

Fig. 7. The drain current (I_d) and gate current (I_g) versus drain voltage (V_{ds}) characteristics of the InP MESFET.

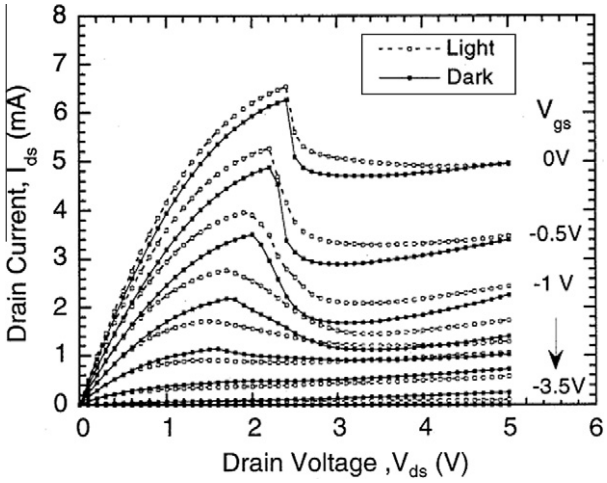

Fig. 8. The transfer characteristic of the InP MESFET with and without illumination, respectively.

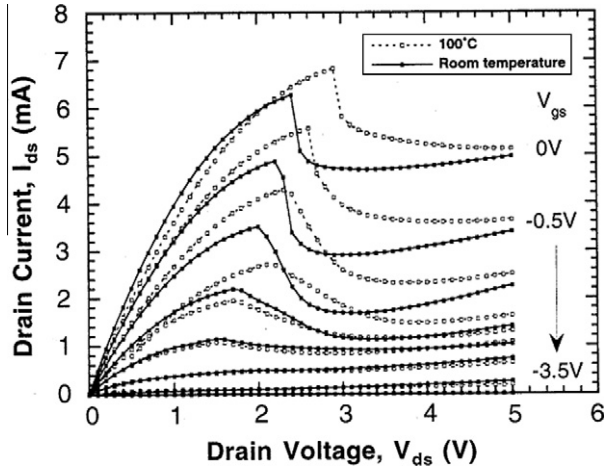

Fig. 9. The transfer characteristic of the InP MESFET which measured at room temperature and 100 °C, respectively.

drain voltage which it reaches the depletion to reach i-InP layer is unchanged.

Fig. 9 shows the transfer characteristics of the device measured at the environment of room temperature and of 100 °C, respectively. The thermal effect agitated more electrons in the n-InP layer and the i-InP layer. So, the heated sample has higher carrier concentration in the active channel layer. Owing to the higher carrier concentration, it needs higher drain voltage to deplete the n-InP layer for the same gate bias. For the curve of $V_{gs} = 0$ V, the voltage on which depleted the n-InP layer increased from 2.4 V to 2.9 V, and the drain current on this point increased from 6.27 mA to 6.82 mA. The device characteristics of the illumination effect and temperature effect give the aid of the explanation of the negative resistance effect was occurred from the stack-layered conduction channel structure.

4. Conclusion

A new n-channel depletion-mode InP field-effect transistor with enhanced barrier height gates, by using Pt/Al double metal is implemented. The device shows characteristics with excellent pitch off, and transconductance of 93 mS/mm. The conductive channel is constituted by a stacked-layered structure, a n-InP layer and an i-InP layer. This results in a negative resistance effect on the MESFET. The device shows good stability with little drain current drift after bias testing.

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