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IMPLEMENTATION OF SWITCHED RELUCTANCE MOTOR DRIVE SYSTEM USING DIGITAL FPGA SCHEME

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ABSTRACT

This paper presents a digital anti-windup IP controller using a field programmable gate array (FPGA) device to improve the dynamic performance of the switched reluctance motor (SRM). Traditionally, the PI controller is designed for operating in the linear region. The windup phenomenon will occur when the output of the PI controller is saturated. The proposed method is then developed to reduce the degradation in the system performance due to saturation. When the output of the IP controller is saturated, the integral state is reset to zero with a rate of the integral time constant by negatively feeding back the controller output. The dynamic characteristics of overshoot, settling time, and load disturbance rejection can then be improved. In addition, the proposed SRM based drive system was implemented by using a digital FPGA scheme to improve the drawback of the analog circuit method. Comparisons have been made to the conventional IP and anti-windup PI controllers. Results show that the proposed anti-windup IP controller outperforms the others methods in terms of overshoot, settling time, and load disturbance rejection.

Key words: anti-windup, switched reluctance motor, field programmable gate array.

I. INTRODUCTION

The switched reluctance motor (SRM) has the advantages of simple structure, robust performance, and low manufacturing cost when compared to the widely used dc motor. However, the SRM still has some unsolved problems, such as the higher torque ripple due to its doubly salient structure, the acoustic noise, and the saturated flux that may limit its applications in high-performance motor drive systems.

Much research has been devoted to coping with the techniques for torque-ripple minimization of SRM. In [1], a balanced commutator was designed to allow accurate current tracking and then reduce the torque ripple over a reasonable operating speed. In [2], a hybrid torque-ripple-minimizing controller is presented along with the simulation and experimental results. The intelligent methods, such as neural network and fuzzy logic [3]-[4], were also presented to solve the torque-ripple problem of the SRM. All of the above techniques have been proposed as practical solutions to the problem of torque ripple for SRM.

In addition to the techniques of torque-ripple minimization, some researchers are also devoted to improve the torque performance of the SRM. These techniques include rotating vector methods for smooth torque control [5], variable structure approach for robust speed control [6], sliding-mode observer for position and speed estimation [7], and the reduction of mutual saturation effect to improve torque performance [8].

In this paper, an alternative approach is developed to implement the SRM drive system. Since the SRM is designed for operating in the saturation region, the torque performance is needed to be promoted by the

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designers. To achieve good dynamic performance and provide a good disturbance rejection, an anti-windup IP controller for SRM is then employed based on the FPGA scheme.

The windup phenomenon occurs when the output of the PI controller is saturated. Therefore, the anti-windup scheme is usually designed to reduce the degradation in the system performance due to saturation. Since the parameters of the PI controller are normally designed in the linear region, the anti-windup strategies, in earlier research, were presented for PID controllers [9]. Recently, a modified anti-windup scheme combining the use of back-calculation and conditional integration techniques is presented to overcome the presence of a significant dead time in the process [10]. To enhance the computational capability and improve the speed response, a digital anti-windup PI controller using the FPGA scheme and stochastic theory has been presented for variable-speed motor drives [11].

This paper, however, presents a digital anti-windup IP controller using a FPGA device to improve the torque performance of the SRM. When the output of the IP controller is saturated, the integral state is reset to zero with a rate of the integral time constant by negatively feeding back the output of the controller. The overshoot, settling time, and the load disturbance rejection can then be improved by the proposed method. In addition, the digital implementation of an anti-windup IP controller using the FPGA scheme has the advantages of reducing circuit complexity, reconfiguring circuits easily, implementing hardware directly, and not being influenced by temperature when compared to the traditional analog circuit method.

II. MATHEMATICAL MODEL

When neglecting the hysteresis loss, eddy current loss, and mutual inductance between windings, the electrical equation of the SRM for each phase is given as

$$E(t) = Ri(t) + \frac{d\lambda(t)}{dt} \tag{1}$$

where $E(t)$ is the instantaneous voltage, $i(t)$ is the instantaneous current, $R(t)$ is the phase resistance, and λ is the instantaneous flux linkage. The electromagnetic dynamic model for the SRM and load can be expressed as follows:

$$T_e(\theta, i) = J\frac{d^2\theta}{dt^2} + B\frac{d\theta}{dt} + T_L \tag{2}$$

where T_e is the electromagnetic torque, J is the inertia constant of the rotor or the connected load, B is the viscous friction coefficient, and T_L is the load torque.

Besides, according to the law of the conservation of energy, the instantaneous torque produced by a single phase is given by

$$T_e = \frac{\partial W_C(\theta, i)}{\partial\theta}\Big|_{i=\text{constant}} \tag{3}$$

where $W_C(\theta, i)$ is the coenergy, which is defined by

$$W_C(\theta, i) = \int_0^i \lambda\, di \tag{4}$$

The other expression of instantaneous torque is given by

$$T_e = -\frac{\partial W_f(\theta, i)}{\partial\theta}\Big|_{i=\text{constant}} \tag{5}$$

where $W_f(\theta, i)$ is the field energy, which is defined by

$$W_f(\theta, i) = -\int_0^i \lambda\, di \tag{6}$$

If the saturation effect is neglected, the relationship between flux leakage λ and current i can be given as

$$\lambda = L(\theta)i \tag{7}$$

where $L(\theta)$ is the inductance of the SRM, which varies with different rotor position as shown in Fig. 1. Equation (7) reveals that the relationship between λ and i is linear. Substituting (7) into (4) and (6) we have

$$W_C(\theta, i) = \frac{1}{2}L(\theta)i^2 = -W_f(\theta, i) \tag{8}$$

Substituting (8) into (3) yields

$$T_e = \frac{1}{2}i^2\frac{dL(\theta)}{d\theta} \tag{9}$$

Figure 2 shows the electromagnetic torque and inductance varied with different rotor position. In practice, the electromagnetic torque is not proportional to the

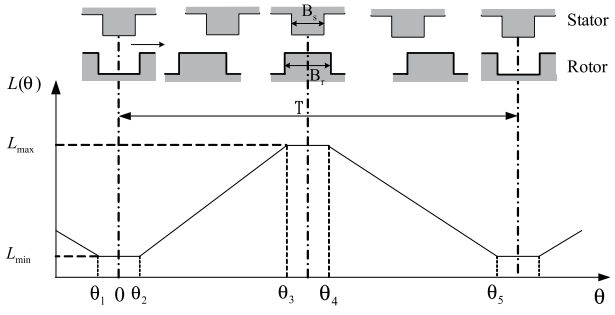

Fig. 1 Motor inductance with different rotor positions.

square of the current due to the saturation phenomenon. Therefore, equation (9) shall be modified to correspond with practical conditions.

III. THE DRIVE SYSTEM OF SRM

According to (7) and Fig. 2, the positive electromagnetic torque can be produced while the phase current is excited at the positive slope of inductance. When the slope of inductance is negative, the opposite electromagnetic torque is provided. But if the phase current is excited at the zero slope of inductance, the rotor will be locked.

The drive system was developed with a three-phase SRM constructed with twelve stator poles and eight rotor poles as shown in Fig. 3. Figure 4 depicts the drive system of the SRM. Each phase consists of two power transistors and one freewheel diode. Such a drive system provides the path of energy discharge while one phase is turned on.

IV. THE PROPOSED APPROACH

This paper proposes the FPGA based anti-windup IP controller to achieve a better performance of the motor drive system. Fig. 5 depicts the block diagram of the proposed method. In Fig. 5, the left-side block is the FPGA based software structure, while the right-side block is the hardware structure. The proposed closed-loop control strategy includes external-loop speed-feedback control and inner-loop current-feedback control. For the external-loop speed-feedback control, the sensor of the rotor position detects the rotor signal and sends it to the speed estimation module which provides the actual speed of the SRM for closed-loop speed control. For the inner-loop current-feedback control, the commutation logic receives the signals of rotor position and judges which phase (A, B, or C) is turned on. Then the switch selects the signal of excited phase current and compares it with the current command obtained from the speed controller to obtain the difference of current signals which will be further sent to the current controller to carry out the inner-loop current-feedback control. Details of the proposed method are described in the following subsections.

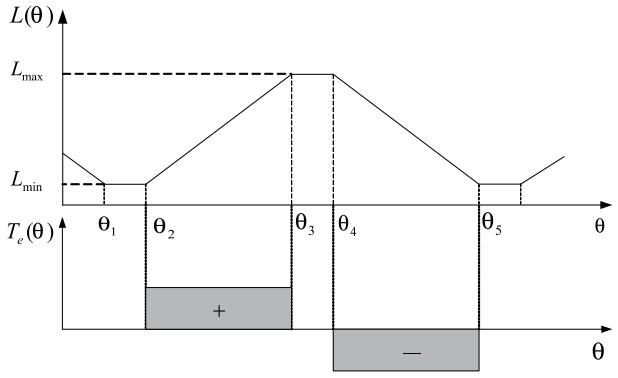

Fig. 2 Electromagnetic torque and inductance with different rotor position.

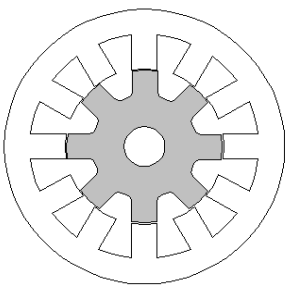

Fig. 3 The structure of the SRM used in this paper (12/8 poles).

4.1 The IP Controller

To describe the difference between PI and IP controllers, schematics of these two controllers are depicted in Fig. 6. The PI controller has a proportional as well as an integral term in the forward path; while the IP controller moves the proportional term to the feedback path and it acts like feedback compensation. Compared with the PI controller, the IP controller has the advantages of a smaller overshoot and faster settling time for both step response and load-variation response [12].

4.2 The Proposed Anti-windup IP Controller

Since the SRM is designed for operating in the saturation region, the windup phenomenon will occur if the traditional PI or IP controller is adopted. To further improve the performance of the IP controller, the anti-

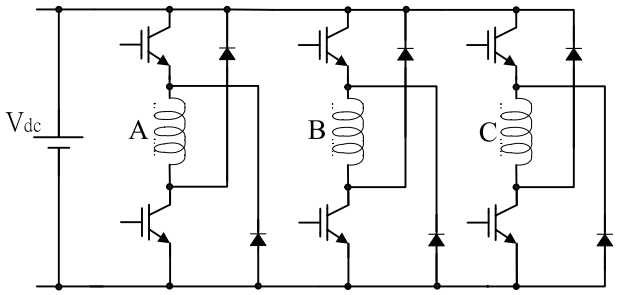

Fig. 4 The three-phase drive system of SRM.

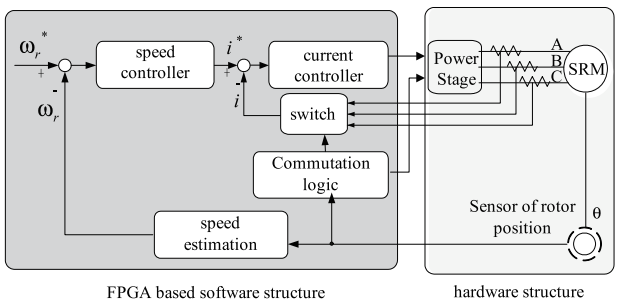

Fig. 5 Block diagram of the proposed method.

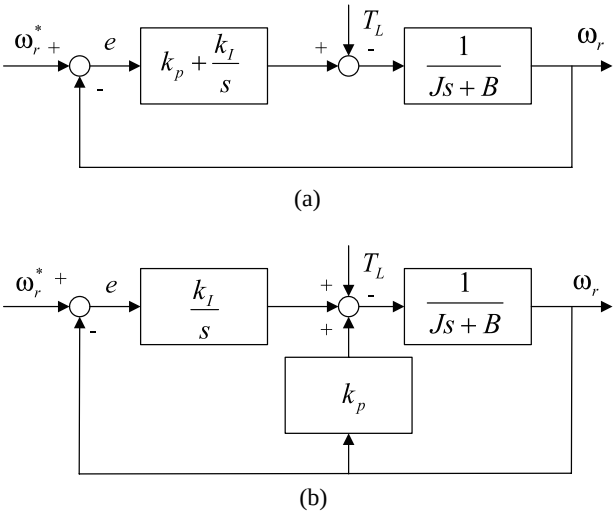

Fig. 6 Schematics of (a) PI controller and (b) IP controller.

windup IP controller based on the FPGA scheme has been presented in this paper.

For the variable-speed control system, if the bandwidth of the current controller is greater than the bandwidth of the speed controller by over ten times, the current dynamics can be neglected. Therefore, the variable-speed control of the SRM shown in Fig. 7 can be modeled as a first-order system as follows.

$$\dot{\omega}_r = -\frac{1}{\tau_m}\omega_r + \frac{k_T}{J}v - \frac{T_L}{J} \tag{10}$$

where ω_r is the motor speed, $\dot{\omega}_r$ is the differential of ω_r, τ_m is the mechanical time constant(=J/B), v is the plant input, and k_T is the torque constant.

As depicted in Fig. 7, the plant input v is limited nonlinearity as follows:

$$v = \begin{cases} u_{\max}, if & u > u_{\max} \\ u, & if \quad u_{\min} \le u \le u_{\max} \\ u_{\min}, if & u < u_{\min} \end{cases} \tag{11}$$

where u_{min} and u_{max} denote the lower and upper bound of u, respectively. The output of the IP controller u can be expressed as

$$u = w - k_P\omega_r \tag{12}$$

where k_p is the proportional gain of IP the controller and w is the integral state. When the speed command or the external load has a large step change, the output of the IP controller u may be saturated. This induces that the plant input is clamped at a prescribed maximum value and the integral state may rapidly converge to zero. Otherwise, the integral state will accumulate the speed error and the IP action is activated. The integral state w can be expressed as follows.

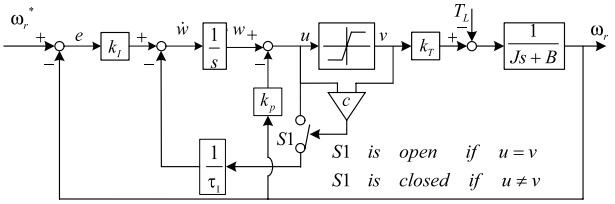

Fig. 7 Schematic diagram of the proposed anti-windup IP controller.

$$\dot{w} = \begin{cases} k_I e & , if \quad u = v \\ k_I e - \dfrac{1}{\tau_I}u & , if \quad u \neq v \end{cases} \tag{13}$$

where k_I denotes the integral gain and τ_I represents the integral time. From (13), it implies that the IP controller is saturated if $u \neq v$, and linear if $u=v$. Equation (13) also assumes that mechanical time constant τ_m is much slower than integral time τ_I.

4.3 Stability Conditions

As shown in (11), the speed controller is operated in either the saturated region or in the linear region. When operating in the saturated region, the anti-windup control strategy will assure that the IP controller can converge toward the linear region. Hence, it is desired to characterize both the domain of attraction when the IP controller is saturated and the asymptotic stability in the linear region.

A. Attractivity Condition

In order to derive the stable condition from saturation to linear, we first define the speed error e as follows:

$$e = \omega_r^* - \omega_r \tag{14}$$

Using (10), it follows that:

$$\dot{e} = -\dot{\omega}_r = -\frac{1}{\tau_m}e - \frac{k_T}{J}v + \frac{1}{\tau_m}\omega_r^* + \frac{T_L}{J} \tag{15}$$

When operating in the saturation region, the dynamics of integral state w can be written as

$$\dot{w} = k_I e - \frac{1}{\tau_I}(w - k_p\omega_r) \tag{16}$$

Let $k_I=k_P/\tau_I$, we have

$$\dot{w} = -\frac{1}{\tau_I}w + \frac{k_p}{\tau_I}\omega_r^* \tag{17}$$

Since $\tau_m >> \tau_I$, the integral state is much faster than that

of the speed error dynamics. Hence, the integral state w can be neglected and the output of the IP controller in (12) can be rewritten as

$$u = -k_P \omega_r = k_P e - k_P \omega_r^* \tag{18}$$

According to (18), there exists a boundary of speed error E_b, which defines the operating domain of the IP controller, and can be expressed as

$$E_b = \frac{u_{\max} + k_P \omega_r^*}{k_P} = \frac{u_{\max}}{k_p} + \omega_r^* \tag{19}$$

Note that if $|e| > E_b$, the IP controller will operate in the saturation region. Otherwise, the IP controller will operate in the linear region.

Now, consider the Lyapunov function

$$V(e) = \frac{1}{2} e^2 \tag{20}$$

The stability condition is satisfied when $\dot{V}(e) \le 0$. Differentiating (20) yields

$$\dot{V}(e) = e\dot{e} = -\frac{1}{\tau_m} e^2 + e\left(-\frac{k_T}{J} v + \frac{1}{\tau_m} \omega_r^* + \frac{T_L}{J} \right) \tag{21}$$

Substituting (15) into (21) yields

$$\begin{aligned} \dot{V}(e) &= -\frac{1}{\tau_m} e^2 + e \frac{k_T}{J} u_{\max} + e\left\{ \frac{1}{\tau_m} \omega_r^* + \frac{T_L}{J} \right\} \\ &\le -\frac{1}{\tau_m} |e|^2 + |e| \left\{ \frac{k_T}{J} u_{\max} + \frac{1}{\tau_m} |\omega_r^*| + \frac{|T_L|}{J} \right\} \end{aligned} \tag{22}$$

To satisfy the stability condition, the absolute speed error e can be expressed as

$$|e| \ge \frac{k_T}{B} u_{\max} + |\omega_r^*| + \frac{|T_L|}{B} \tag{23}$$

Aggregating Eqs.(19) and (23), and satisfy the condition of $|e| < E_b$, the attractivity condition can be expressed as

$$|T_L| < \left(\frac{B}{k_p} - k_T \right) u_{\max} \tag{24}$$

B. Asymptotic Stability Condition

When the IP controller operates in the linear region, the IP action is activated and the speed error is accumulated. It follows using (15) that the speed error equation can be expressed as

$$\dot{e} = -\left(\frac{1}{\tau_m} + \frac{k_T k_p}{J} \right) e - \frac{k_T}{J} w + \left(\frac{1}{\tau_m} + \frac{k_T k_p}{J} \right) \omega_r^* + \frac{T_L}{J} \tag{25}$$

To acquire the asymptotic stability condition, the Lyapunov function is used and given by

$$V(e, w) = \frac{1}{2} \frac{J}{k_T} e^2 + \frac{1}{2} \frac{\tau_I}{k_p} (w - w_{ss})^2 \tag{26}$$

where w_{ss} is the steady-state of integral state w and the gain of k_p is positive. The time derivative of Lyapunov function can then be written as

$$\begin{aligned} \dot{V}(e,w) = &-\frac{J}{k_T} \left(\frac{1}{\tau_m} + \frac{k_T k_p}{J} \right) e^2 \\ &+ e \left\{ \left(\frac{J}{k_T \tau_m} + k_p \right) \omega_r^* + \frac{T_L}{k_T} - w_{ss} \right\} \end{aligned} \tag{27}$$

In general, the integral state will have an adequate value w_{ss} given by

$$w_{ss} = \frac{J}{k_T} \left\{ \left(\frac{1}{\tau_m} + \frac{k_T k_p}{J} \right) \omega_r^* + \frac{T_L}{J} \right\} \tag{28}$$

When the term $\dot{V}(e,w)$ in (27) is less or equal to zero, the stable condition in the linear region is then satisfied. But in the saturation region, w_{ss} must be less than u_{max}. The asymptotic stability condition can therefore be obtained as follows:

$$\left(\frac{1}{\tau_m} + \frac{k_T k_p}{J} \right) |\omega_r^*| + \left| \frac{T_L}{J} \right| \le \frac{k_T}{J} u_{\max} \tag{29}$$

or

$$\left(B + k_T k_p \right) |\omega_r^*| + |T_L| \le k_T u_{\max} \tag{30}$$

If the operating conditions satisfy the inequality in (30), even if the IP controller output is saturated, the error dynamics can still asymptotically converge in the linear region.

4.4 Design Methods

For a step speed command r, such that $|r| \le E_b$, the closed-loop transfer function $U(s)/R(s)$ in the linear region can be expressed as

$$\frac{U(s)}{R(s)} = G(s) = \frac{k_p \left(\frac{1}{\tau_I} s + \frac{1}{\tau_I \tau_m} \right)}{s^2 + \left(\frac{k_p k_T}{J} + \frac{1}{\tau_m} \right) s + \frac{k_p k_T}{\tau_I J}} \tag{31}$$

To keep the speed error in the linear region, the output of the IP controller must be less than the limitation of the plant input u_{max}. From (19), the following equation can be obtained

$$k_p |r| |G(s)| \le k_p \left(E_b - \omega_r^* \right) \tag{32}$$

where the transfer function $G(s)$ must satisfy：

$$|G(j\omega)| \le 1, \qquad \forall \omega \tag{33}$$

We now consider a second-order function given by

$$\frac{U(s)}{R(s)} = G(s) = \frac{b_2 s^2 + b_1 s + b_0}{a_2 s^2 + a_1 s + a_0} \tag{34}$$

where a_x and b_x are real values. When $U(j\omega) \le R(j\omega), \forall \omega$, the transfer function must satisfy the condition given in (33). Therefore,

$$|G(j\omega)|^2 = \frac{\left(b_0 - b_2\omega^2\right)^2 + b_1^2\omega^2}{\left(a_0 - a_2\omega^2\right)^2 + a_1^2\omega^2} \le 1 \tag{35}$$

Rearrange inequality in (35), the relation between a_x and b_x can be expressed as

$$|a_2| \ge |b_2|, \qquad |a_0| \ge |b_0|, \qquad a_1^2 - b_1^2 - 2(a_0 a_2 - b_0 b_2) \ge 0 \tag{36}$$

Comparing (31) with (34), the stability region of k_p and τ_I can be obtained as follows:

$$\tau_I \ge \frac{k_p J}{\sqrt{\left(k_p k_T + B\right)^2 + k_T^2} - k_T} \tag{37}$$

4.5 The FPGA based Scheme

The FPGA is composed of many integrated circuits that provide the basic functions of combinational logic and sequential logic. Through the connection of each logic cell by vertical channel and horizontal channel, the FPGA can carry out some useful functions designed by the users. In this paper, the FPGA based scheme is employed to construct the digital anti-windup IP controller for the SRM system. Figure 8 illustrates the FPGA scheme of the proposed anti-windup IP controller. The scheme is implemented in an Altera FPGA chip using Max+pulse II software. In addition, the numerical representation of the data uses the floating-point method. The precision of the circuit depends on the definition of the parameters. If the parameters are expressed only with decimal component, then its precision can be reached at 2^{-15}.

As shown in Fig. 8, the output of the digital integrator can be expressed as

$$y(n) = x(n) + y(n-1) \tag{38}$$

where $x(n)$ is the input of the digital integrator and $y(n\text{-}1)$ is the register output. Note that the register holds the previous output of the integrator and sends the one-step time-delayed output signal back to the adder to perform the integration function. The comparator is served as a limiter which limits the signal level within the lower and upper bounds. When the output of controller exceeds the boundaries, the comparator will output a signal to the multiplexer to hold on boundary values. In the meantime, the output of the comparator enables the negative-feedback function of $1/\tau_I$. On the other hand, if the output of controller doesn't exceed the boundaries, the output of comparator is the same as the controller output and the negative-feedback function of $1/\tau_I$ will be disabled.

Figure 9 depicts the schematic diagram of FPGA based scheme, which can be summarized in the following steps:

Step 1 Initialize the related devices.

Step 2 Detect the rotor position and output the commutation signal.

Step 3 Check if the current exceeds the rated value? If it is true, disable the commutation output; otherwise, proceed to the next step.

Step 4 Execute the current-feedback control. Repeat steps 3 to 4 until they are executed five times.

Step 5 Check if the current is saturated. If it is true, perform the proposed anti-windup IP control; otherwise, proceed to execute the traditional IP control.

Step 6 Update current command and proceed to step 2.

To exhibit the proposed FPGA scheme, simulations on the FPGA circuit were implemented. Figure 10 shows the simulation signals of positive commutation logic, where A1, A2, B1, B2, C1, and C2 are gate drive signals and S0, S1, and S2 are rotor position signals. The system clock used in the FPGA scheme is 10 MHz. Figure 11 reveals the simulation results of the current-feedback and speed-feedback controllers. As shown in the figure, the sampling time of current loop and speed loop are

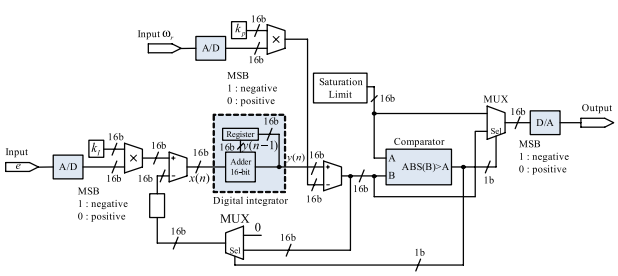

Fig. 8 The FPGA scheme of the proposed anti-windup IP controller.

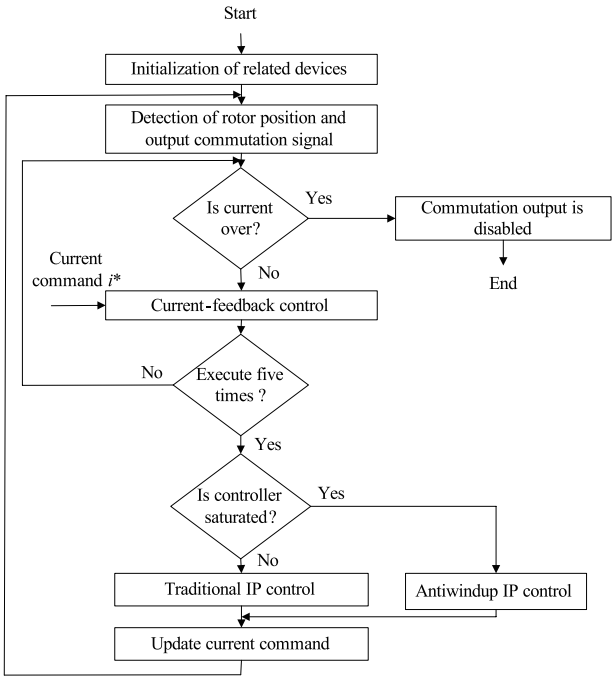

Fig. 9 The schematic diagram of the FPGA based anti-windup IP controller.

102.4μs (OSC1) and 512μs (OSC3) respectively. When the speed command (Wr_COM) is set at 1800 rpm and the actual speed (Wr) fed back from the motor is 1600 rpm, the current command (I_COM) can then be estimated by the speed controller. The obtained current command (84 or 3.36A) is compared with the actual current (Current) and acquires the controller output (C_OUT) of 293 via the current controller, which means the current controller will output 28.6% duty cycle of PWM to the drive system of the SRM. By following the above processes, the closed-loop control strategy of FPGA scheme can be accomplished.

V. THE EXPERIMENTAL RESULTS

As shown in Fig. 5, the structure of the proposed method comprises of two phases: hardware and software. The hardware phase consists of the SRM, power stage, FPGA modules, and interface circuits, while the software phase contains commutation logic, speed estimation, current controller, and speed controller. Table 1 shows the specifications for the SRM used in this paper. Table 2 reveals the execution time and sampling time for both current-feedback and speed-feedback controllers. Since the bandwidth between current loop and speed loop is different, the sampling time of the speed- feedback controller is set to five times of the current-feedback controller.

To verify the performance of the proposed method, experiments of step response and load variation are implemented. Comparisons of the proposed method with other methods are also made in this section.

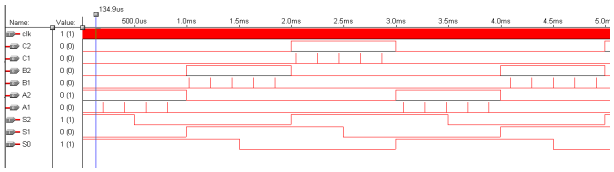

Fig. 10 Simulation signals of positive commutation logic.

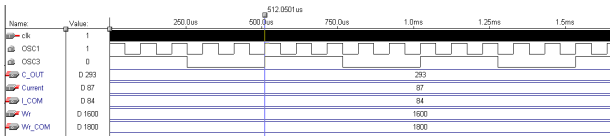

Fig. 11 Simulation results of current-feedback and speed-feedback controllers.

Table 1 The specifications for SRM used in this paper.

Number of stator poles	12
Number of rotor poles	8
Rated capacity	120V, 2.5A
Rated speed	1500 rpm
Range of speed	100 ~ 2000 rpm
Overload capability	1.1 times of rated capacity

Table 2 Execution time and sampling time for each controller.

	Execution time	Sampling time
Current-feedback controller	Each time while counters interrupt	102.4μs (9.765kHz)
Speed-feedback controller	Once while current-feedback controller executes five times	512.0 μs (1.953kHz)

A. Step-Response Experiment

For the step-response experiment, the transfer function from the current loop to the speed loop is 1250/(s+0.893). The parameters of rise time t_r, damping ratio ζ, and the other parameters such as k_{Iv}, k_{pv}, and k_I are listed in Table 3.

Figures 12 and 13 show the responses of speed and current commands for different controllers at 1000 rpm and 1800 rpm respectively. The windup phenomenon occurs at 1800 rpm. Table 4 shows the performance criteria of each controller, including rise time, overshoot, settling time, and steady state error. Experimental results obtained from windup and non-windup cases reveal that the proposed anti-windup IP control method can provide superior performances such as no overshoot, faster settling time, and better steady state error than the other control methods.

Table 3 The setting of each parameter.

Methods	Parameters				
	t_r	ζ	k_{Iv}	k_{pv}	τ_I
IP controller	0.4	0.975	0.862	0.0505	0.1500
Anti-windup PI controller	0.4	0.800	0.867	0.0126	0.1533
Anti-windup IP controller	0.4	0.975	0.862	0.0505	0.0383

Notes: t_r: Rise time; ζ : Damping ratio; k_{Iv}: Integral gain; k_{pv}: Proportional gain; τ_I: Integral time

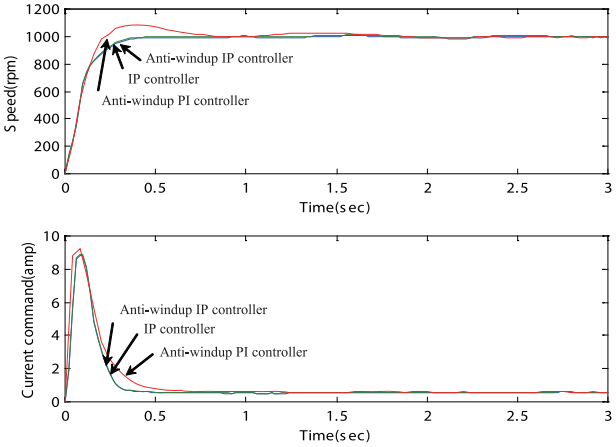

Fig. 12 The speed and current responses at 1000 rpm.

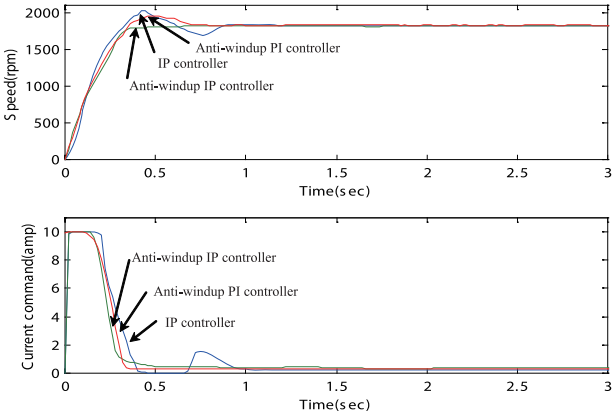

Fig. 13 The speed and current responses at 1800 rpm.

Table 4 Performance comparison of each controller at 1800rpm.

	Performance parameters			
	Rise time	Over-shoot	Settling time	Steady state error
IP controller	0.32s	12.22 %	0.72 s	0.44%
Anti-windup PI controller	0.36s	8.33%	0.88s	0.44%
Anti-windup IP controller	0.33s	0.00%	0.35s	0.00%

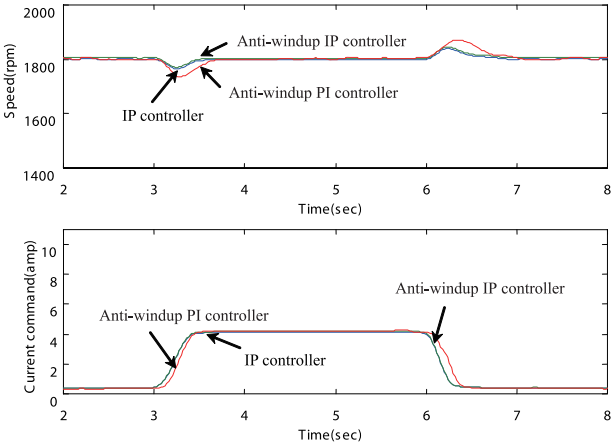

Fig. 14 The speed and current responses with load variation at 1800 rpm.

B. Load-Variation Experiment

To verify the dynamic performance of the proposed method, load-variation experiment was also implemented. Figure 14 depicts the speed and current responses with the load increased and reduced for different controllers at 1800 rpm. The load was increased at t=3s and reduced at t=6s. The experimental results reveal that the proposed anti-windup IP controller has the better performance of load disturbance than the other methods.

VI. CONCLUSIONS

A new technique that combines anti-windup IP controller and the FPGA device to construct a variable-speed SRM system has been presented in this paper. Results from step response and load variation experiments have shown that the proposed method outperforms the other methods in overshoot, settling time, steady-state error, and load disturbance rejection. Besides, compared with traditional analog implementation methods, the proposed FPGA based digital implementation method provides several advantages, such as direct hardware implementation, easy reconfiguration of circuit, and not being influenced by temperature.

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