DTIP 2009 of MEMS & MOEMS, 1-3 April, Rome, Italy

The Development of the High Performance Parallel-Stacked RF Spiral Inductor

D.K. Jair[1], M. C. Hsieh[2], C. S. Lin[3], S. M. Chen[4] and Y. H. Chen[1]

1 Department of Mechanical Engineering, Kun Shan University, Taiwan, R.O.C.
2 Department of Electronic Engineering, Kun Shan University, Taiwan, R.O.C.
3 Department of Electronic Engineering, Fortune Institute of Technology, Kaoshiung, Taiwan, R.O.C.
4 Institute of Microelectronics, National Cheng Kung University, Taiwan, R.O.C.

***Abstract*- In this work, deep sub-micron CMOS process compatible high Q on chip spiral inductors with air- gap structure and parallel stacked inductor have been fabricated with 0.18μm CMOS compatible process. In the design the electromagnetic solver, SONNET, and the finite element program, ANSYS, were used for electrical-characteristics and maximum mechanical strength, respectively. Experimental results show that measured peak Q and peak-Q frequency attain 7.06 and 1.8GHz for the structure of four metal layers parallel and metal width of 15um at 5.5 turns, respectively and 5.2 and 1.6GHz for the suspending spiral inductor. Besides, the experimental results also shows the parallel stacked structure saves the chip area significantly and reduces resistance to obtain high Q value at low frequency significantly.**

I. INTRODUCTION

On-chip inductor has been widely used in integrated radio-frequency (RF) CMOS circuits as on-chip matching network, inductive load, passive filter, transformer, etc. [1]. For these applications, the most issue is the large silicon substrate losses [2], which will limit the performance of inductors at higher frequencies. Research has focussed on improving the Q factor of CMOS inductors by using custom process modules. In the past, many high performance structures on Si substrates have been proposed to overcome this issue [1][2][3]. These include fabrication of inductors with thick copper layers on Saphire substrates, and removal of the underlying silicon by wetetchants. With the continuing reduction of the chip size, the unit-current-gain (f_t) of device in CMOS technology has exceed 10 GHz [4]. Therefore, CMOS technology has been widely used on various CMOS RF applications. However, the poor characteristics of the passive devices, especially the on-chip inductors become the greatest topics in real applications. One of the most important characteristics of the inductor is quality factor (Q). The Q factor significantly affects the performances of the RF circuits and systems, such as the gain/power ratio of the LNA[5], and the phase noise of the VCO[6]. Since the inductors possess poor Q factor due to the substrate loss and higher resistance in RF frequencies. Therefore, to realize high Q on-chip inductor in the standard CMOS process is one of the major challenges for CMOS RF applications. In the past, on-chip inductors include flatness and stacked structures. In a conventional RF on-chip planar spiral inductor that is embraced by the SiO_2, the capacitive and substrate losses can result in interference with other devices through substrate coupling due to its large area, thus making it difficult to integrate a high energy RF power amplifier and a sensitive RF receiver circuit on the same die, because it is necessary to keep each planar on-chip inductor away to lower the substrate coupling noise. Recently, the CMOS process compatible RF inductors with air gap structure and laterally laid out structure were introduced to reduce the substrate loss for obtaining high Q has been reported [7][8]. Although the on-chip air gap inductors possess higher Q, but the structures are suffering to vibrate and complicate process compared with conventional process. With the continuing reduction of the chip size, the metal thickness become more and more thin thus result in the higher resistance which degrade the Q value. The series structure inductors not only have higher resistance but also consume area. It is well known that the lower resistance will promote the Q factor in low frequency [4].

In this paper, on-chip suspended spiral inductor and parallel stacked structure inductors with CMOS process compatible was implemented. We use the mature CMOS technology compatible processing and air gap structure to reduce substrate losses and parallel stacked structure to reduce the resistance, thus can promote the Q factor.

II . DESIGN AND FABRICATION

The samples in this study were prepared by using conventional 0.18μm full eight-level Cu metal/FSG (fluorinated oxide) low-k IMD CMOS process technology on silicon substrate with a field oxide of 0.4um thickness as shown schematically in Fig.1(a) (top view) and Fig.1(b) (side view).

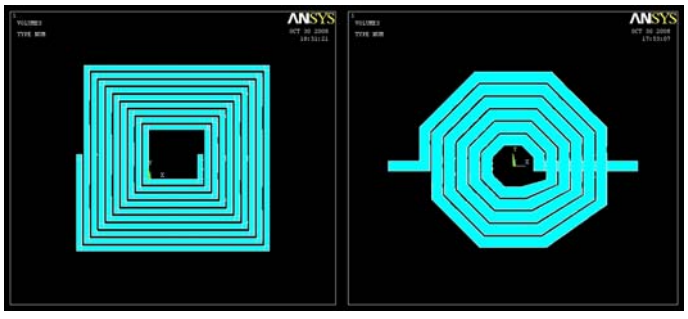

Fig1.(a) The schematic diagram of the on-chip suspended spiral inductor (left) and parallel stacked structure (right)

 ISBN:

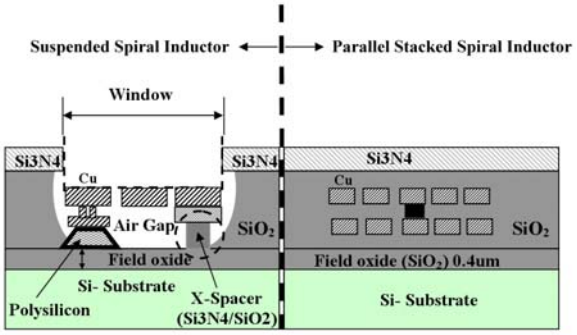

Fig1.(b) The schematic diagram of cross section for the on-chip suspended spiral inductor (left) and parallel stacked structure (right)

After having finished the single layer inductor with a thickness of 1um by dual damascene electroless copper plating with a thickness of 0.9um, the windows of the inductor were opened over the proposed on-chip inductor by removing LPCVD Si_3N_4 (0.1um) and SiO_2 (0.6um) layers on the using the process for the opening of bonding pad window. Then the slope wet etching solutions consists of 107ml DI water, 509ml 10:1 BOE, 35ml 49% HF, and 349ml CH_3COOH per one liter at 25^0C was applied for three minutes to form the air gap, i.e., to remove the SiO_2 embraced the inductor. Next, upper metals with desired pattern were completed using same metalization process. Fig.2 shows the SEM pictures of the completed developed spiral inductors. The dimensions of the proposed suspending spiral inductor are 100um, 10um, 2um and 10 turns for the inner diameter, width, spacing, and number of turns, respectively, while the dimensions of the parallel stacked inductor are 30μm, 3μm, for the inner diameter, and spacing, respectively（Fig.2）

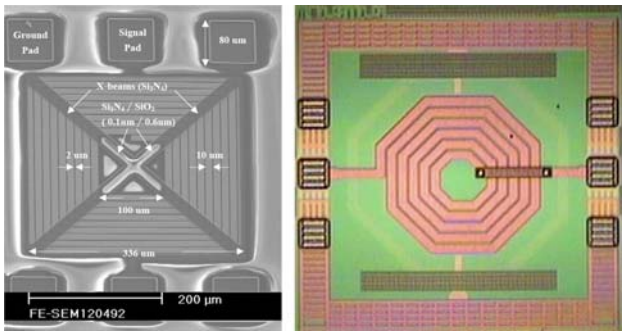

Fig.2 The SEM photos of the on-chip suspended spiral inductor (left) and parallel stacked structure (right)

Finally, the samples were taken to HP 8510C Vector Network Analyzer (VNA) for measurement of S-parameter to obtain Q and Cascade Micro-tech probe station with the Cascade HPC G-S-G (ground-signal-ground) probes are provided to measure S- parameters of device characteristics on wafer from 45MHz to 50GHz. After transforming the measured S-matrix of the total on-chip inductor with periphery components and periphery components itself into the Y-matrix, respectively, the $Y_{de\text{-}embbed}$ that represents the desired Y-matrix of DUT can be obtains by the subtracting the periphery components out as follows.

$$Y_{de-embbed} = Y_{DUT} = Y[S_{total}] - Y[S_{periphery}]$$

All the parameters in the Ashby's lump circuit model at a fixed frequency can be extracted from $Y_{de\text{-}embbed}$. For example, the Y_{11} can be derived approximately as following:

$$Y_{11} = \frac{1}{jwL_s + R_s} + jwC_f$$

and the reciprocal of Y_{11} is

$$\frac{1}{Y_{11}} = \frac{R_s}{(1-w^2L_sC_f)^2 + (wR_sC_f)^2_{3)}} + jw\frac{L_s - (w^2L_s{}^2C_f + R_s{}^2C_f)}{(1-w^2L_sC_f)^2 + (wR_sC_f)^2}($$

The L_s and R_s at low frequency (200 MHz) can be derived as following:

$$L_s = -\frac{\mathrm{Im}\left\{\frac{1}{Y_{11}}\right\}}{2\pi f}$$

And

$$R_s = \mathrm{Re}\left\{\frac{1}{Y_{11}}\right\}$$

and the C_f can be extracted from the frequency f_0 where $|Y_{21}|$=0:

$$C_f = \frac{1}{(2\pi f_0)^2 L_s}$$

After decision of R_s, L_s, and C_f, the parameters of the other elements can be obtained from simulation by tuning fine fitting curves such as S-parameters in smith chart, plots of Q, L_s, and R_s between the model and de-embedding data of the same inductor. The Q factor is the main parameter to determine the quality of an inductor and its general definition is expressed in [1-3]. Result from the stored energy is proportional to the imaginary part of the Z_{in} and the dissipated energy is proportional to the real part of the Z_{in}, the Q factor can be extracted from the de-embedding Y-parameters expressed as following:

$$Q = \frac{-\mathrm{Im}\left[\frac{1}{Y_{11}}\right]}{\mathrm{Re}\left[\frac{1}{Y_{11}}\right]} = -\frac{\mathrm{Im}[Y_{11}]}{\mathrm{Re}[Y_{11}]}$$

The substrate resistivity is 2 K ohm-cm. The using of high resistivity substrate is to reduce conducting losses of substrate and thus raising quality factor (Q) [10].

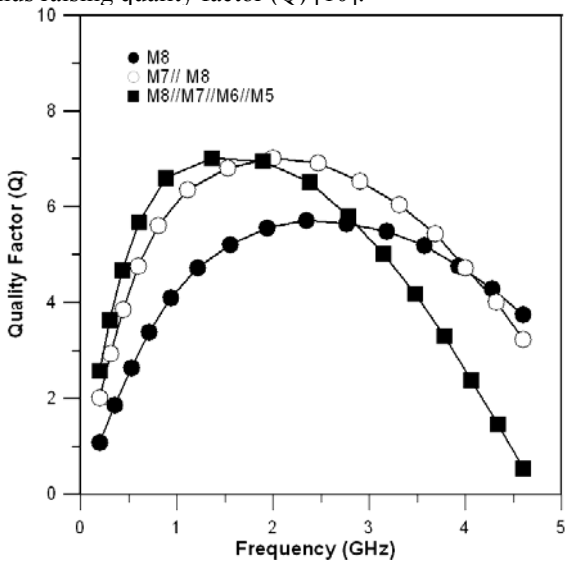

Fig.3 Measured Q inductance as a function of frequency for the different parallel metal layers

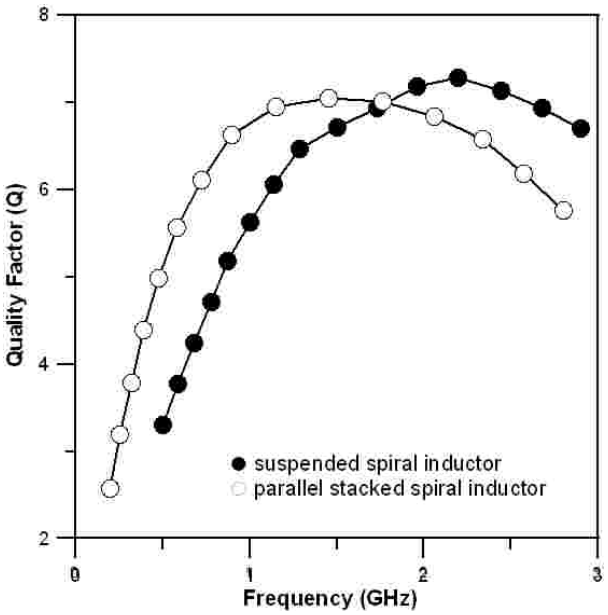

Fig.4 The quality factor of the suspended spiral inductor and the parallel-stacked structure

III. Result and Discussion

Fig.3 presents the measured Q as a function of frequency for the different parallel metal layers with the number of turns, radius, spacing and metal width of 5.5 turns, 30um, 3um, and 15um, respectively. From the Fig.3, the peak Q value increases with increasing the parallel layer numbers. This is because of the reduction of resistance which promotes the quality factor at low frequency. A comparison of the quality factor of the suspended spiral inductor and the parallel-stacked structure is shown in fig.4. The measured maximum Q and peak-Q frequency for maximum Q of suspended spiral inductor and parallel-stacked structure are 7.3, 2.1GHz and 7.06, 1.8GHz, respectively. Since the dimensions of the suspending spiral inductor and parallel stacked inductor are about 210×210 um^2, 117×117 um^2, respectively. The chip area can be reduced significantly for the parallel stacked structure and the resistance can be reduced by using the parallel stacked structure thus results in an obviously improving of the Q at low frequency. Furthermore, comparing to the parallel stacked structure, the thickness of suspended spiral inductor's metal wire is very thin (0.4um), so that the mechanical stability of the suspended structure, especially for the inductor with large number of turns, may still be vulnerable or distorted by it's own gravity. The maximum impact force for the parallel stacked structure is much higher than the suspended spiral with air-gap structure [11]. Fig.5 show the measured Q and L as a function of frequency for the parallel stacked inductor with using the top and bottom signal pad with the number of turns, radius, spacing and metal width of 5.5 turns, 30um, 3um, and 15um, respectively. The measured peak Q and peak-Q frequency for top and bottom signal pad are 7.06, 1.8GHz and 6.65, 1.6 GHz. It can be clearly found that the top signal pad structure has lower capacitance between the metal wire and substrate thus increasing the quality factor.

Fig.6 (a) and (b) present the measured Q and inductance as a function of frequency for the 5.5 turns inductor with metal width of 6um, 9um and 15um, respectively. The measured peak Q and peak-Q frequency with metal width of 6um are 6.5 and 6GHz, respectively. The peak Q decrease with increasing the metal width due to the increase of capacitances from the metal layer to the substrate and the fringing capacitance between the upper and lower metal lines.

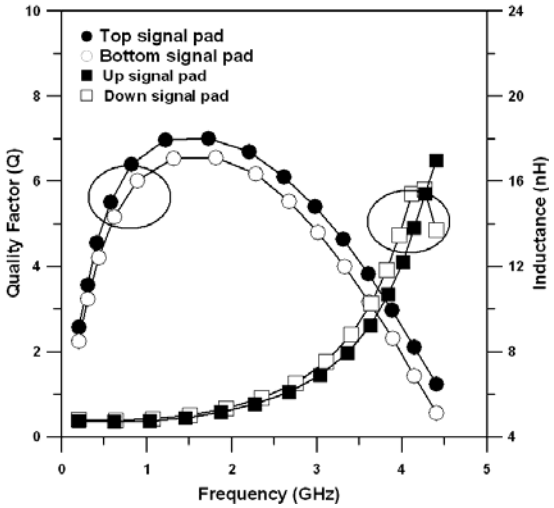

Fig.5 the measured Q and inductance as a function of frequency for the parallel stacked inductor with using the top and bottom signal pad

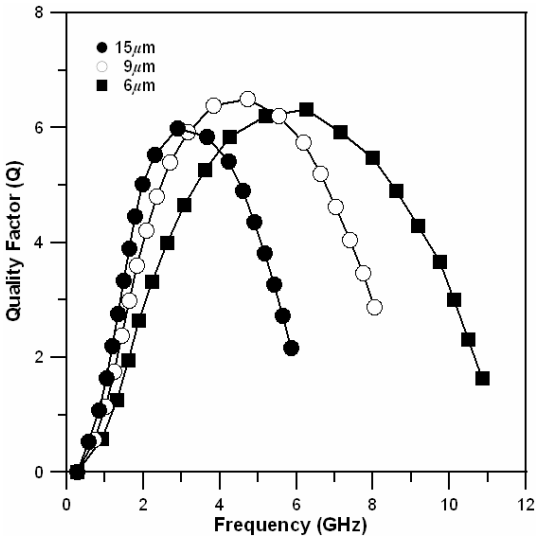

Fig.6 The measured Q as a function of frequency for the 5.5 turns inductor with metal width of 6um, 9um and 15um, respectively.

IV . Summary

In this study, a deep-submicron CMOS process compatible parallel stacked inductor has been successfully developed. Experimental results evidence that by using the parallel stacked structure, the chip area can be reduced significantly for the issue of continuing reduction of the chip size. Furthermore, the resistance can be reduced by using the parallel stacked structure and thus results in an obviously improving of the Q at low frequency. The measured peak Q and peak-Q frequency with the parallel metal layer of M8//M7//M6//M5 are 7.06 and 1.8GHz, thus enhancing its applications for higher frequency RF IC. Therefore, the developed deep-submicron CMOS process compatible parallel stacked inductor is suitable for CMOS RF integrated circuit applications.

ACKNOWLEDGMENT

The work was financially supported by the National Science Council under contract NSC 97-2221-E-168 -035 –

REFERENCES

[1] Ali M., Niknejad and R. G.. Meyer: "Analysis, Design, and Optmization of Spiral Inductors and Transformers for Si RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 33, no.10, pp.1470 –1481, Oct. 1998.

[2] B. Kirk, A. Koullias, William C. Finley, John J. Bastek, and Shahriar Moinian: "High Q Inductors for Wireless Applications in a Complementary Silicon Bipolar Process," *IEEE Journal of Solid-State Circuits*, vol. 31, no.1, pp. 4-9, Jan. 1996.

[3] Min Park, Seonghearn Lee, Cheon Soo Kim, Hyun Kyu Yu, and Kee Soo Nam: "The Detailed Analysis of High CMOS Compatible Microwave Spiral Inductors in Silicon Technology," *IEEE Transactions on Electron Devices*, vol. 45, no. 9, pp. 1953 –1959, Sept. 1998.

[4] Chih-Chun Tang, Chia-Hsin Wu,, and Shen-Iuan Liu," Miniature 3-D Inductors in Standard CMOS Process", *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 37, NO. 4, APR. 2002

[5] H. Darabi and A. A. Abidi, "A 4.5-mW 900-MHz CMOS receiver for wireless paging," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1085–1096, Aug. 2000.

[6] . Craninckx and M. S. J. Steyaert, "A 1.8-GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors," *IEEE J. Solid-State Circuits*, vol. 32, pp. 736–744, May 1997.

[7] C. S. Lin, Y. K. Fang, S. F. Chen, C. Y. Lin, T. H. Chou,S. M. Chen, M. C. Hsieh," A Novel Ni Capped High Q Copper Air Gap Spiral Inductor", Materials Science in Semiconductor Processing, *Volume 8, Issue 4, Pages 545-549, August 2005*

[8] C. S. Lin, Y. K. Fang, S. F. Chen, C. Y. Lin, M. C. Hsieh, C. M. Lai, T. H. Chou,C. H. Chen,"A Deep Sub-Micron CMOS Process Compatible High Q Air Gap Solenoid Inductor with Laterally Laid Structure", *IEEE ELECTRON DEVICE LETTERS,* Vol. 26, No.3, pp. 160-162,2005

[9] J. Craninckx, M. Steyaert, and H. Miyakawa, "A fully integrated spiral-LC CMOS VCO set with prescaler for GSM and DCS-1800 systems," in *Proc. Custom Integrated Circuits Conf.*, 1997, pp. 403–406.

[10] M. Park, S. Lee, C. S. Kim, H. Kyu, and K. S. Nam, "The detail analysis of high-Q CMOS-compatible microwave spiral inductors in Si technology," *IEEE Trans. Electron Devices*, vol. 45, no. 9, pp. 1953–1959, Sep. 1998

[11] M.C. Hsieh, D.K. Jair, and Y.K. Fang, and C. S. Lin, " Designand fabrication of the suspended high-Q spiral inductors with X - beams," symposium on DTIP2007, stresa, Italy, 25-27 April 2007